

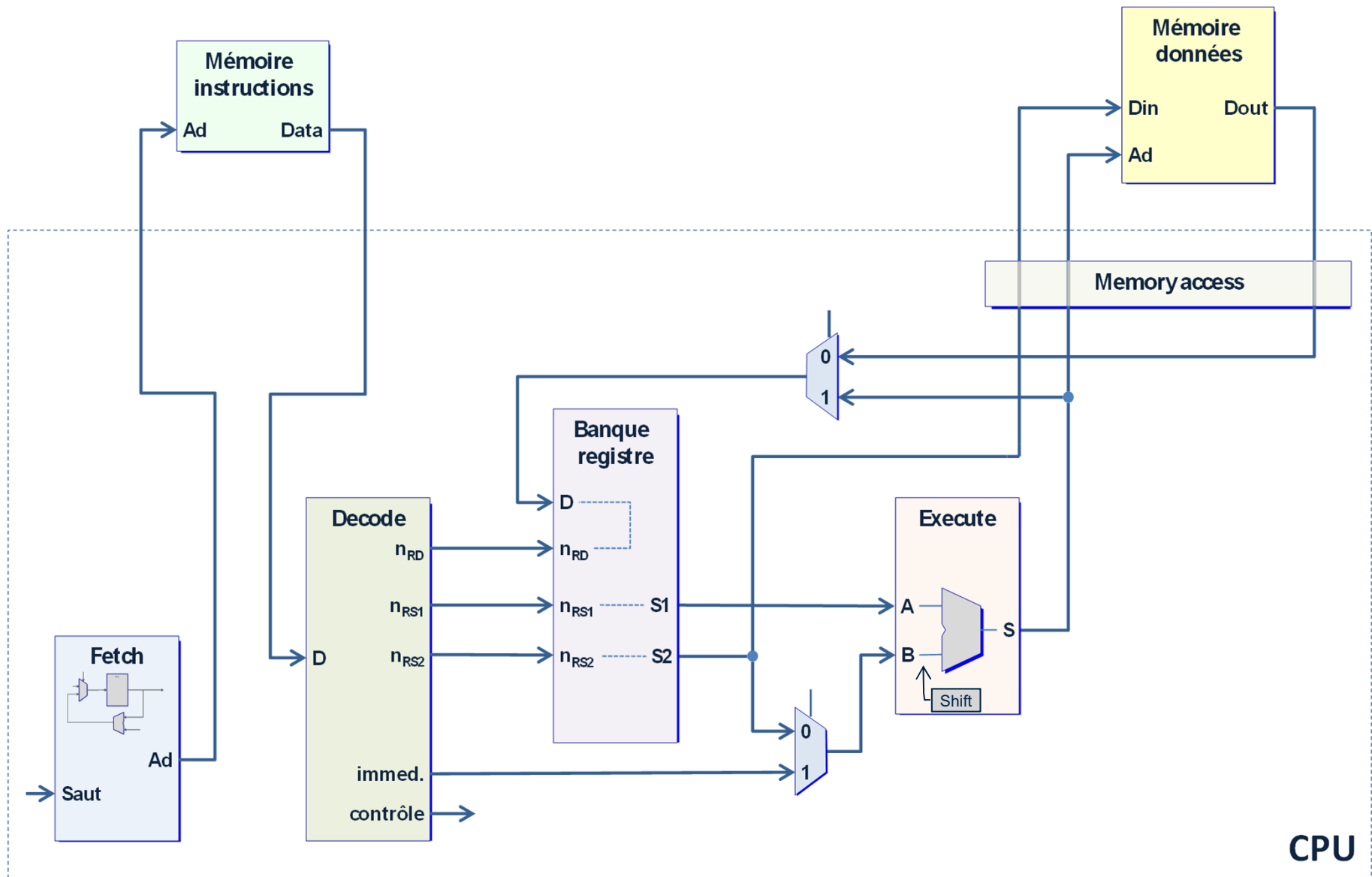
ARO2

Micro-architecture d'un processeur Schéma-bloc global et récapitulatif

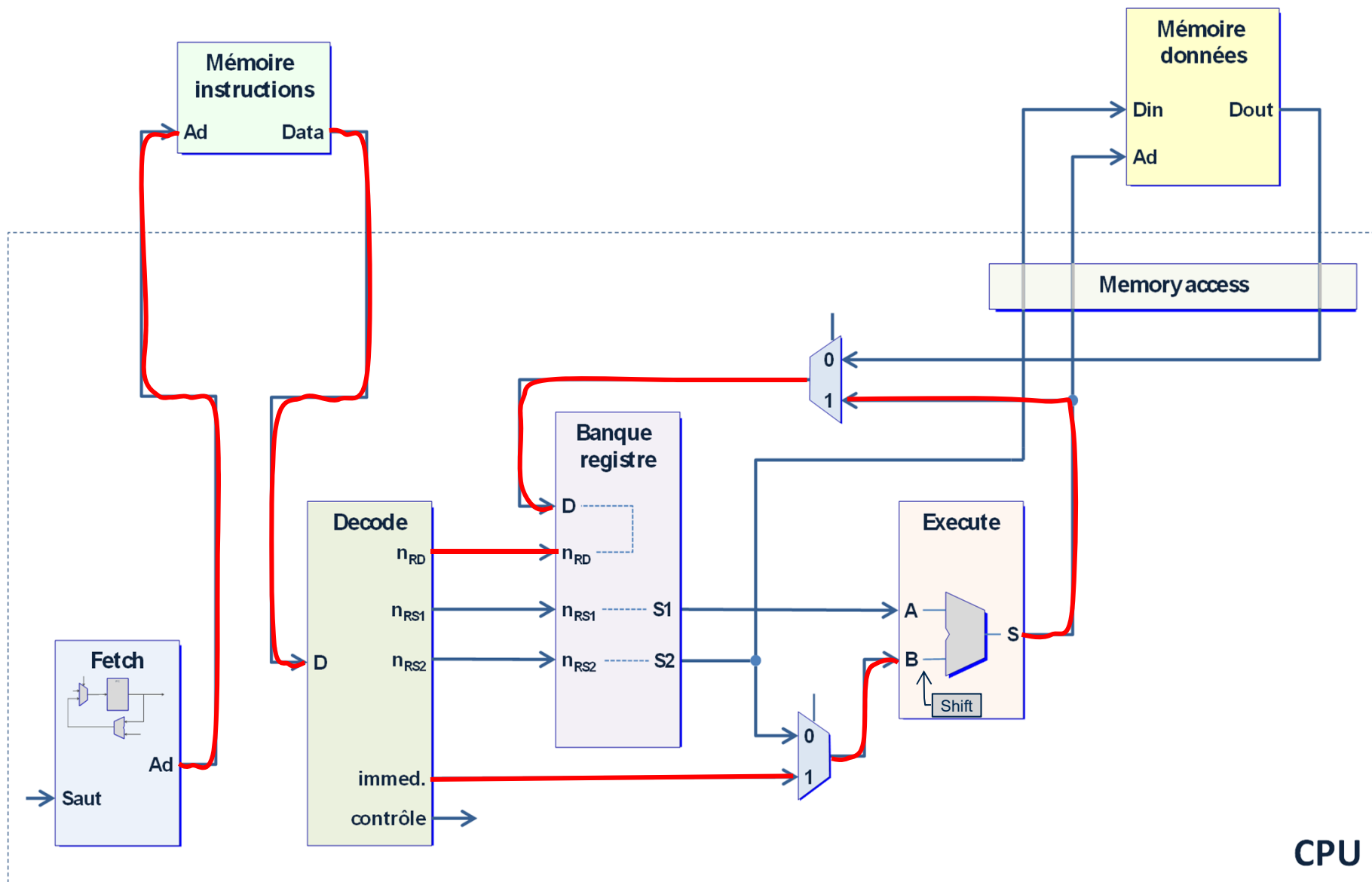
Basé sur le cours du prof. E. Sanchez
et le cours ASP du prof. M. Starkier

Romuald Mosqueron

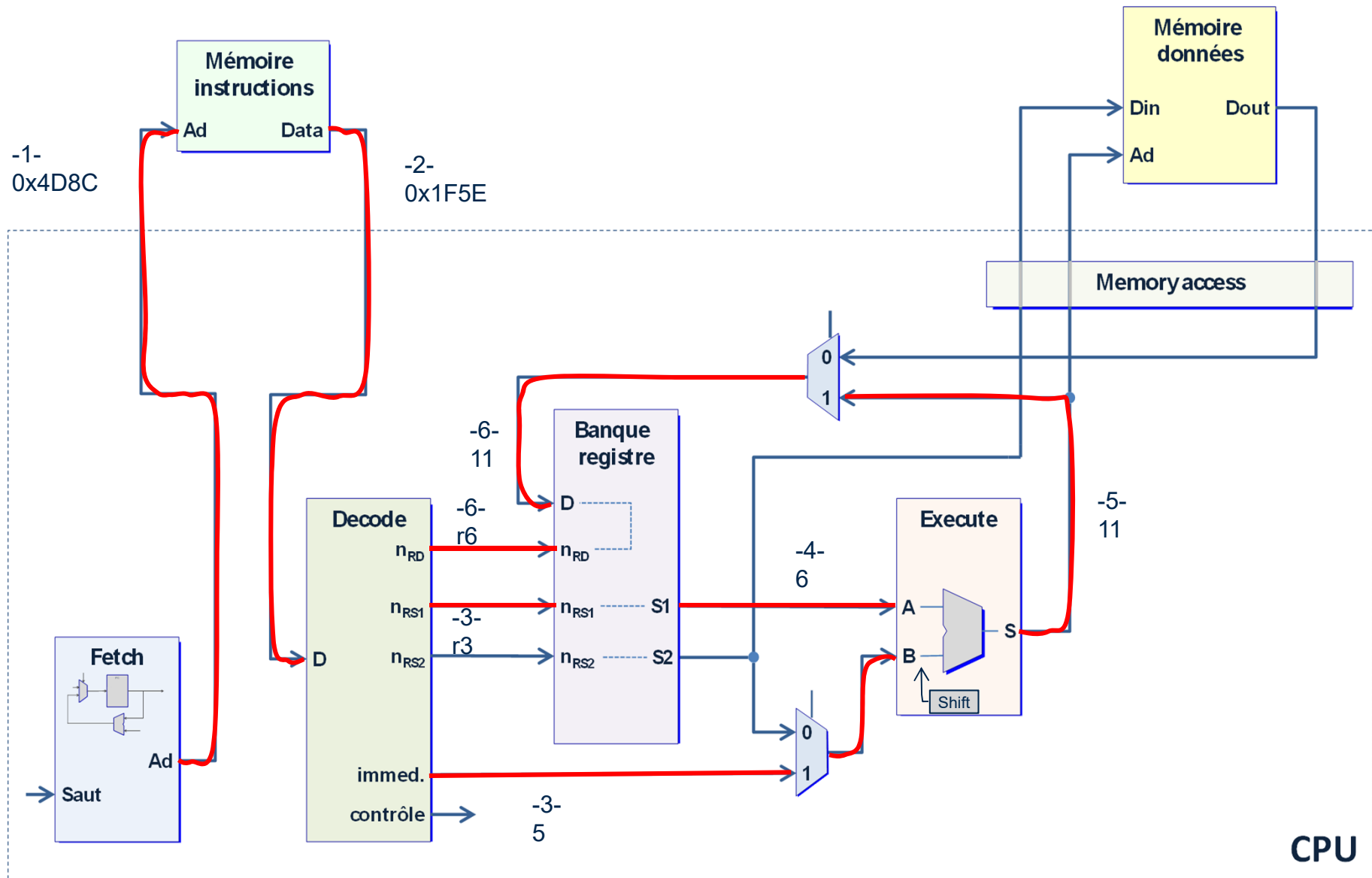
Microarchitecture d'un processeur de type ARM



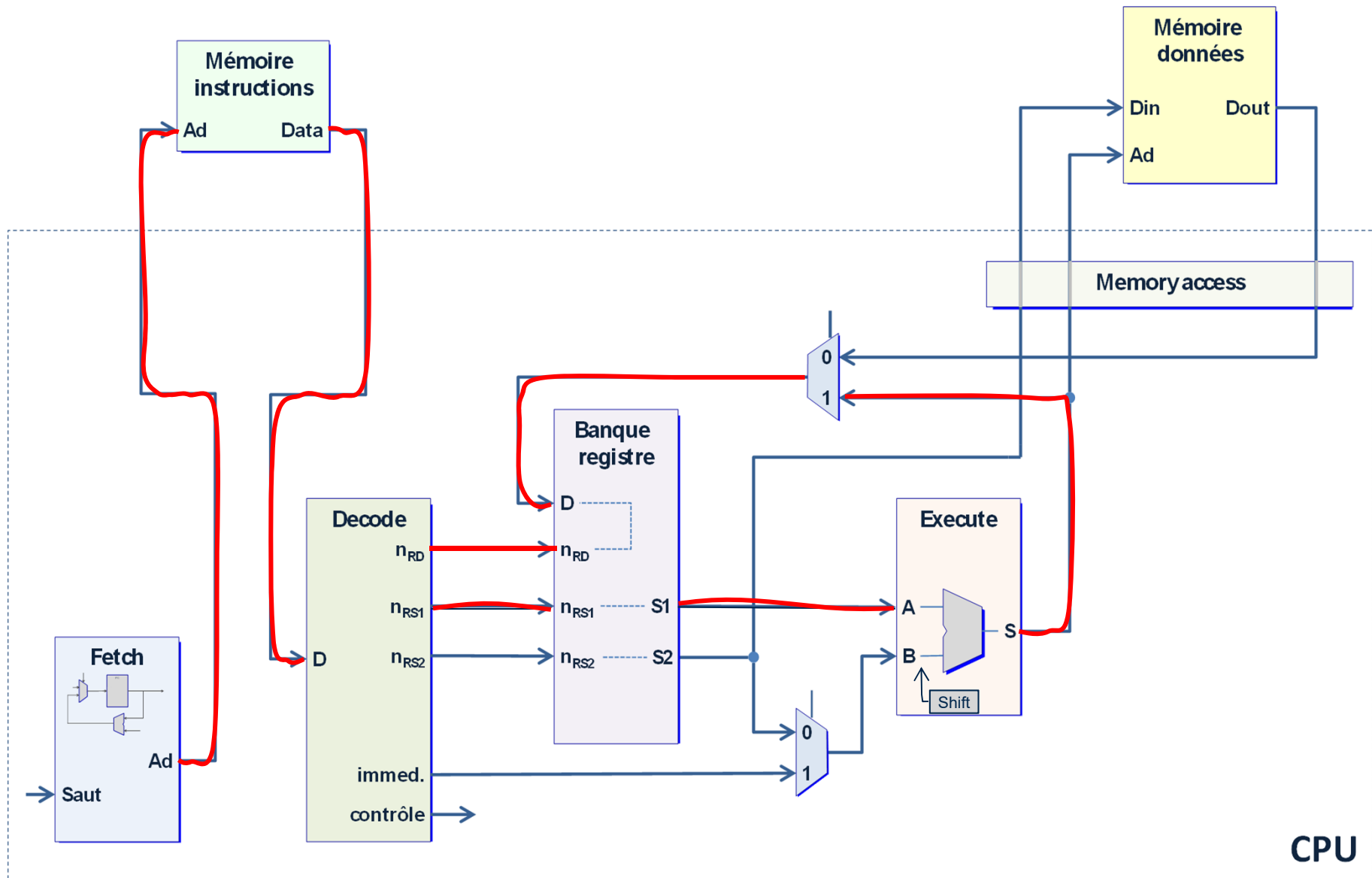
Instruction MOV <Rd>, #<immed_8>



Instruction ADD r6,r3,#5

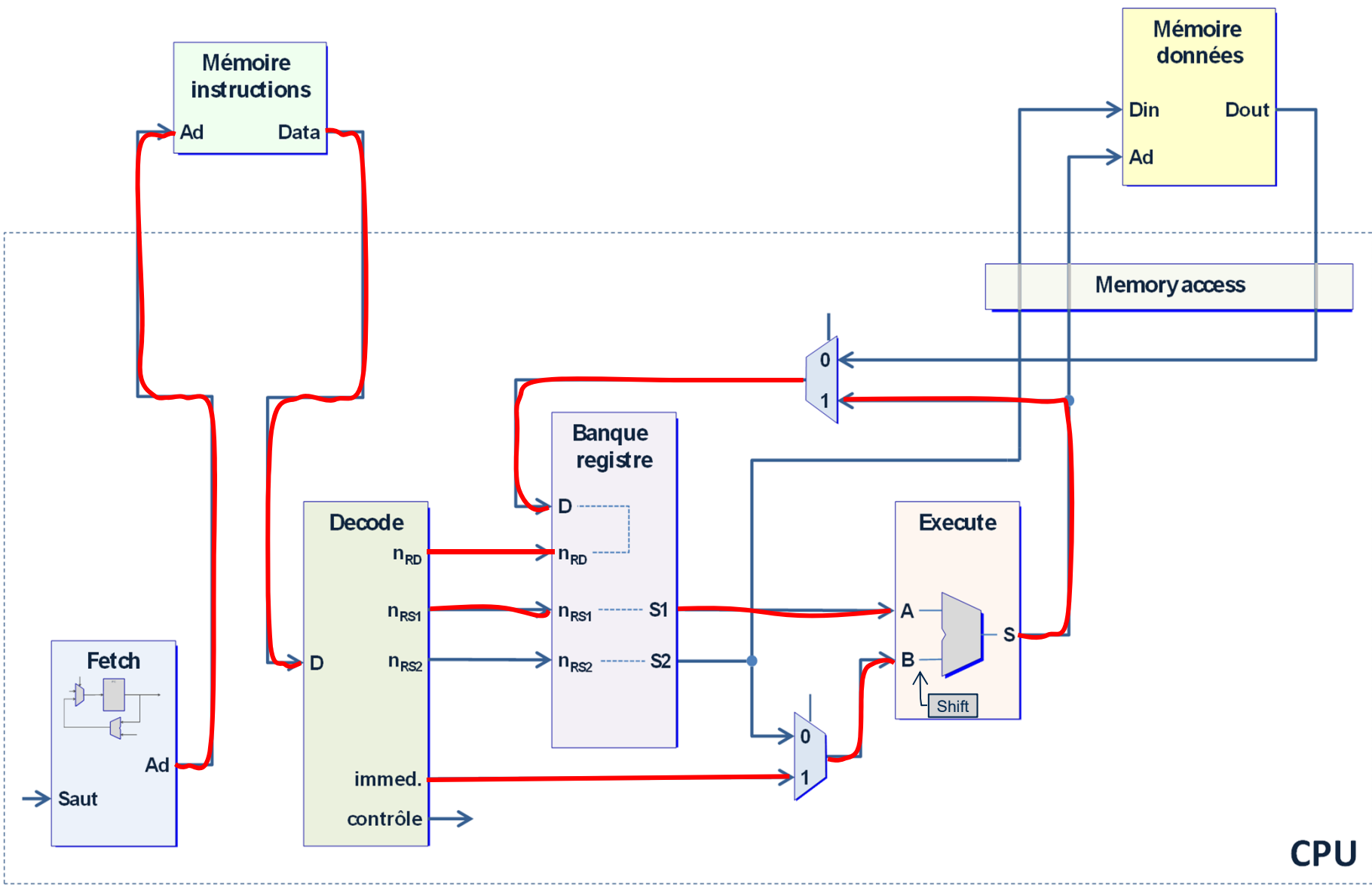


Instruction MOV <Rd>, <Rn>



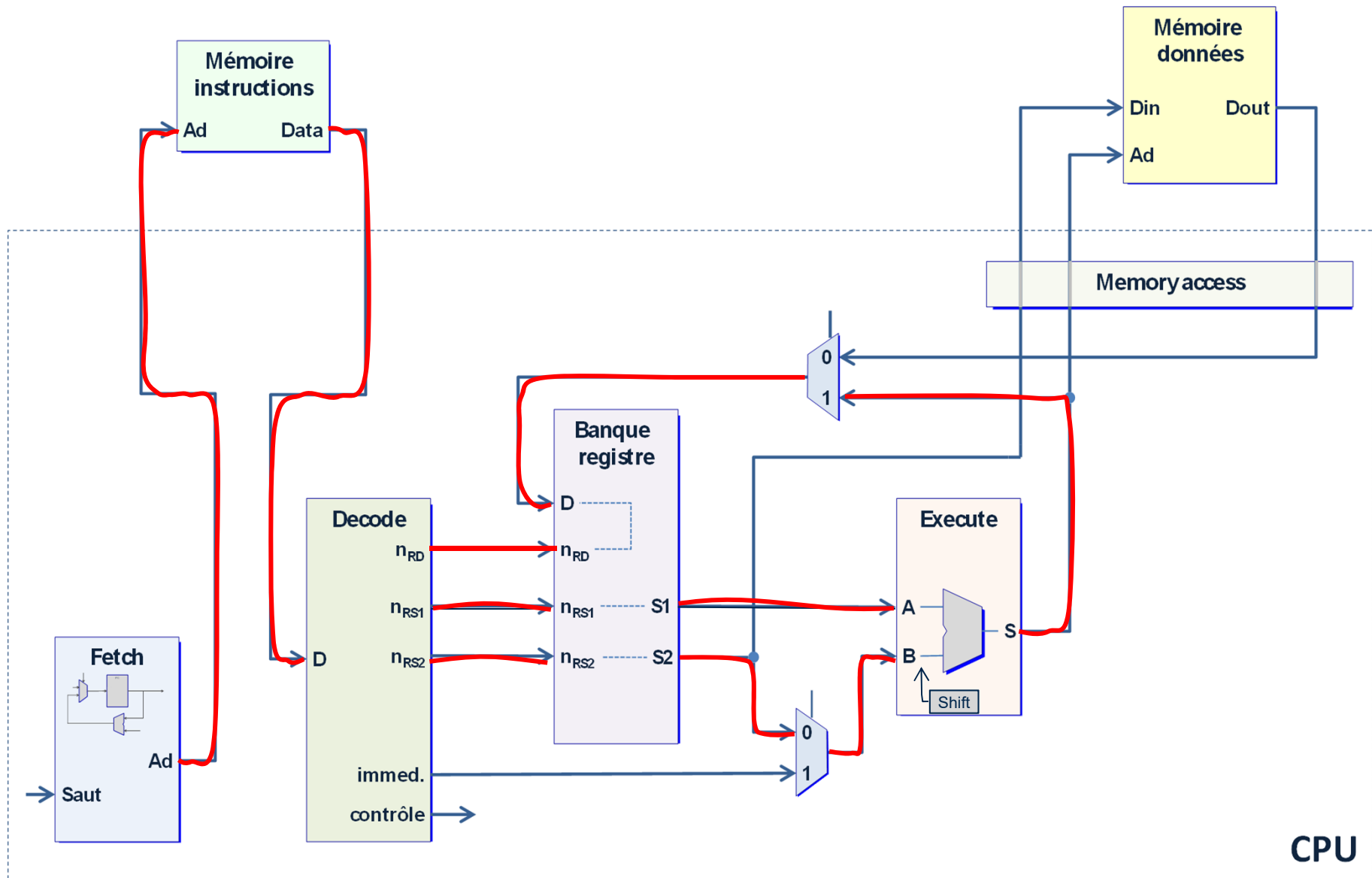
CPU

Instruction ADD <Rd>, <Rn>, #<immed_3>



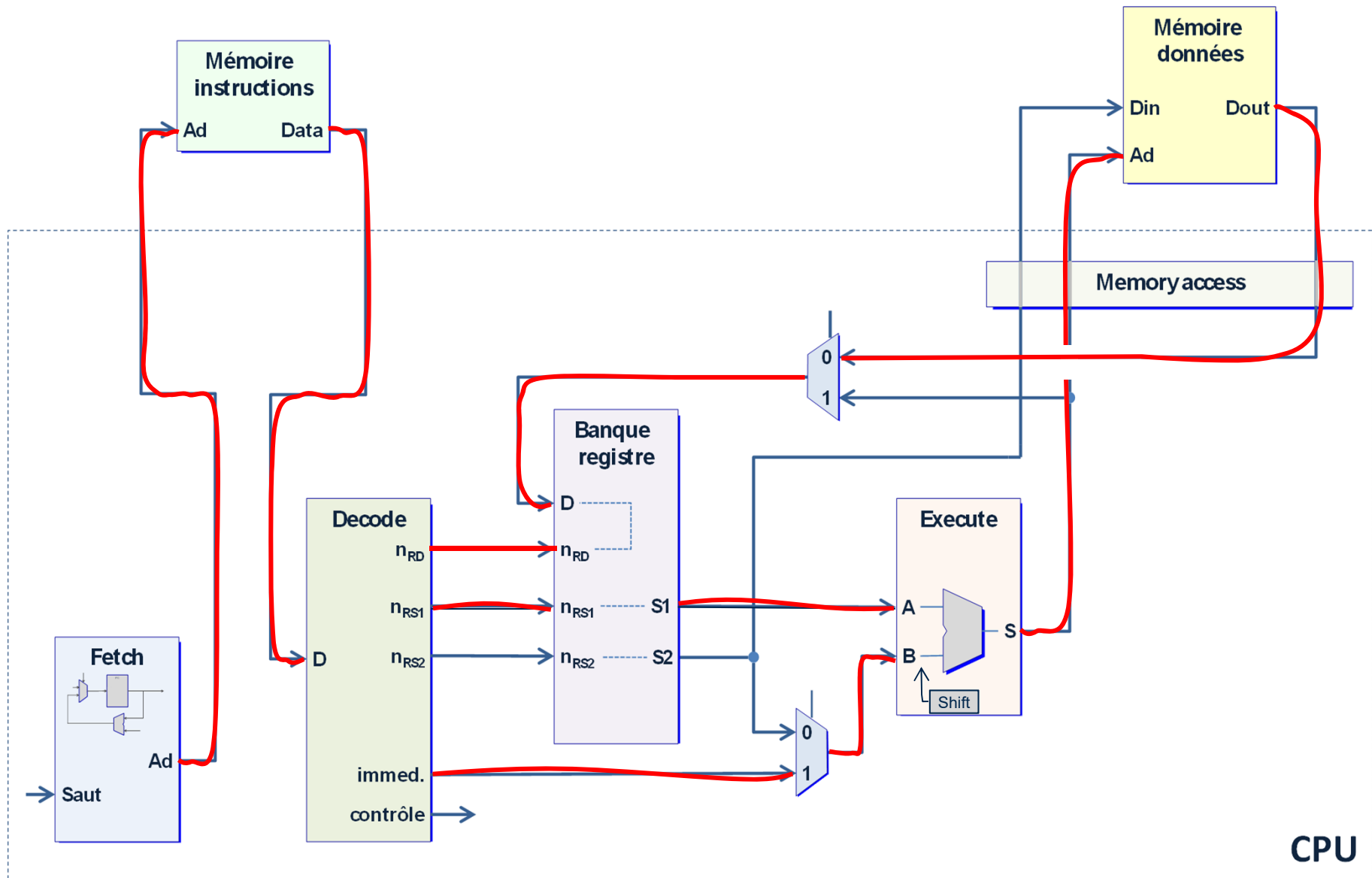
CPU

Instruction ADD <Rd>, <Rn>, <Rm>



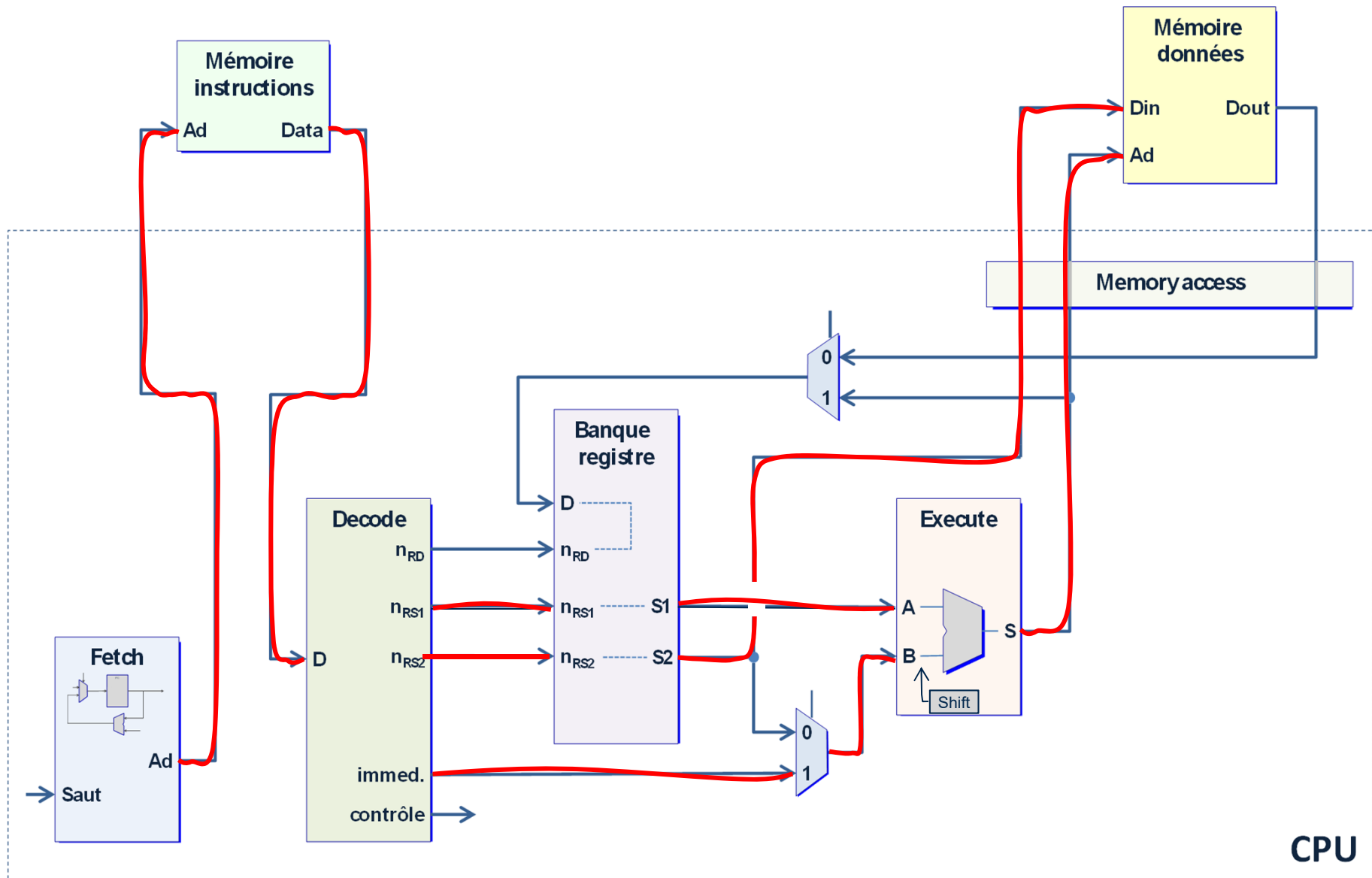
CPU

Instruction LDRH <Rd>, [<Rn>, #<immed_5> * 2]



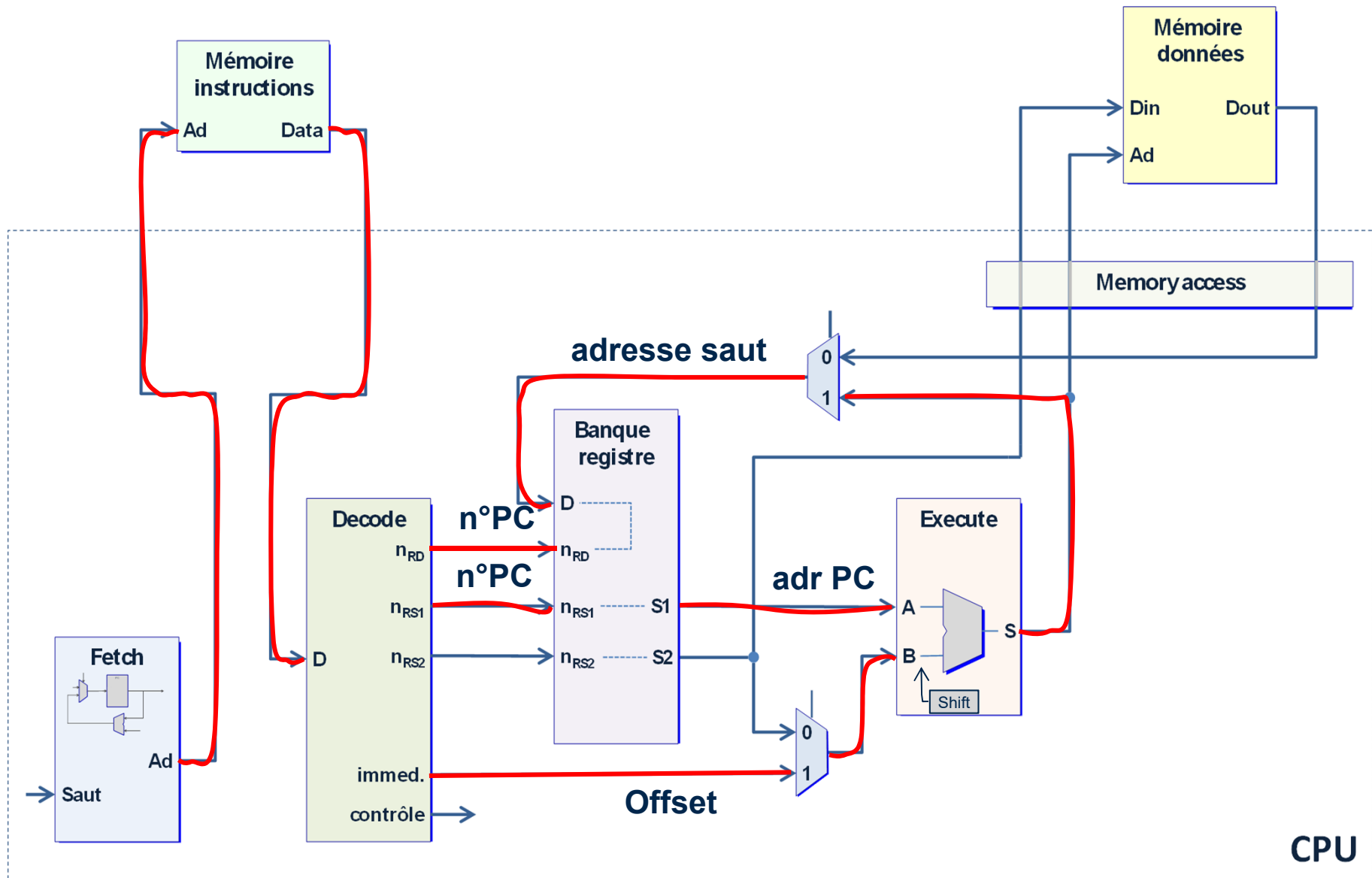
CPU

Instruction STRH <Rd>, [<Rn>, #<immed_5> * 2]



CPU

Instruction B <target_address>



- **Compléter les schémas avec les valeurs correspondant aux exemples ci-dessous :**

Slide 3: MOV R3, #34

Slide 4: R6 = 26, MOV R2, R6

Slide 5: R3 = 12, ADD R2, R3, #3

Slide 6: R4 = 14, R6 = 7, ADD R1, R4, R6

Slide 7: R2 = 0x200, LDRH R3, [R2, #3 * 2]

Slide 8: R6 = 37, R5 = 0x 220, STRH R6, [R5,#4 * 2]

Slide 9: PC = 0x140, Label = 0x150, B Label