Unité IFS (Interface)

Architecture d'un système embarqué & intro plateforme REPTAR

heig-vd
Haute Ecole d'Ingénierie et de Gestion du Canton de Vaud

REDS

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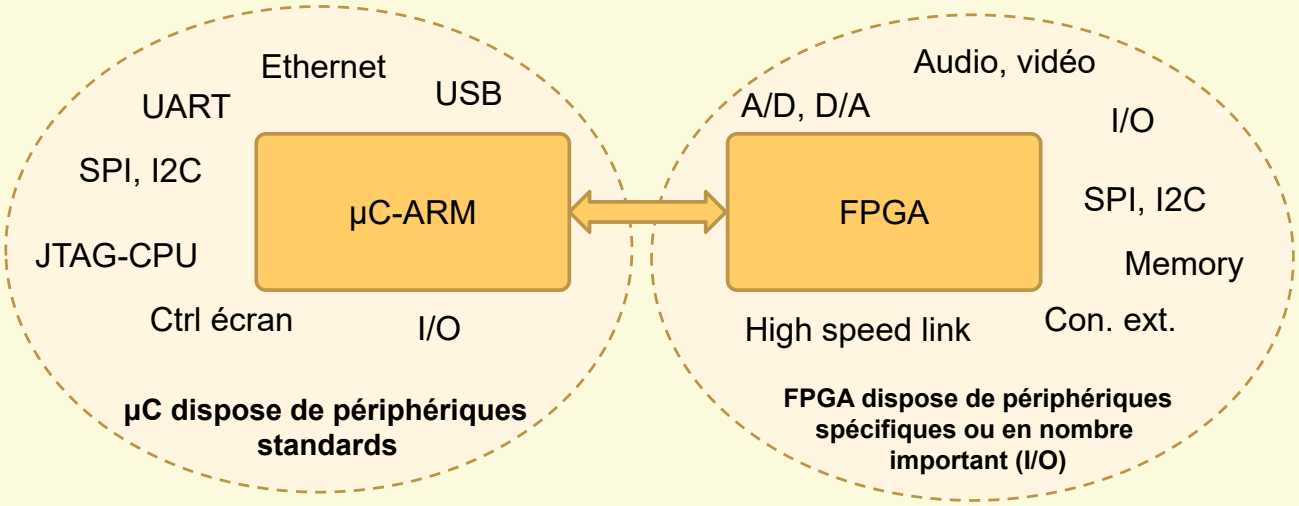
Contenu présentation

- Architecture générale d'un système embarqué
- La plateforme REPTAR
  - Architecture de la plateforme
  - Module µC-DM3730 de la plateforme REPTAR, architecture, plan d'adressage, I/O simples
  - Zone d'adressage pour les mémoires et périphériques externes au µC-DM3730
  - La FPGA Spartan 6, interface local bus, I/Os disponibles

Architecture systèmes embarqués

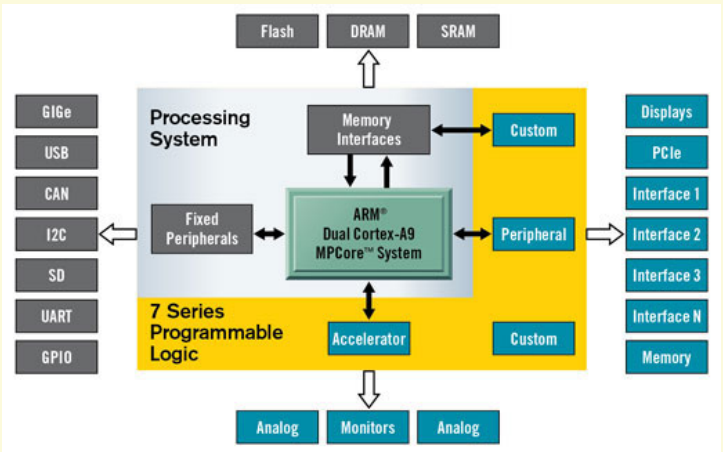
- Architecture utilisée dans le cadre de l'institut REDS pour un système embarqué:
  - plateforme comprend µC-ARM & FPGA



Architecture systèmes embarqués

- Nouveau composant: SoC-FPGA
  - Un boitier comprenant :
    SoC dual core ARM & FPGA

Architecture Zynq-7000 de Xilinx



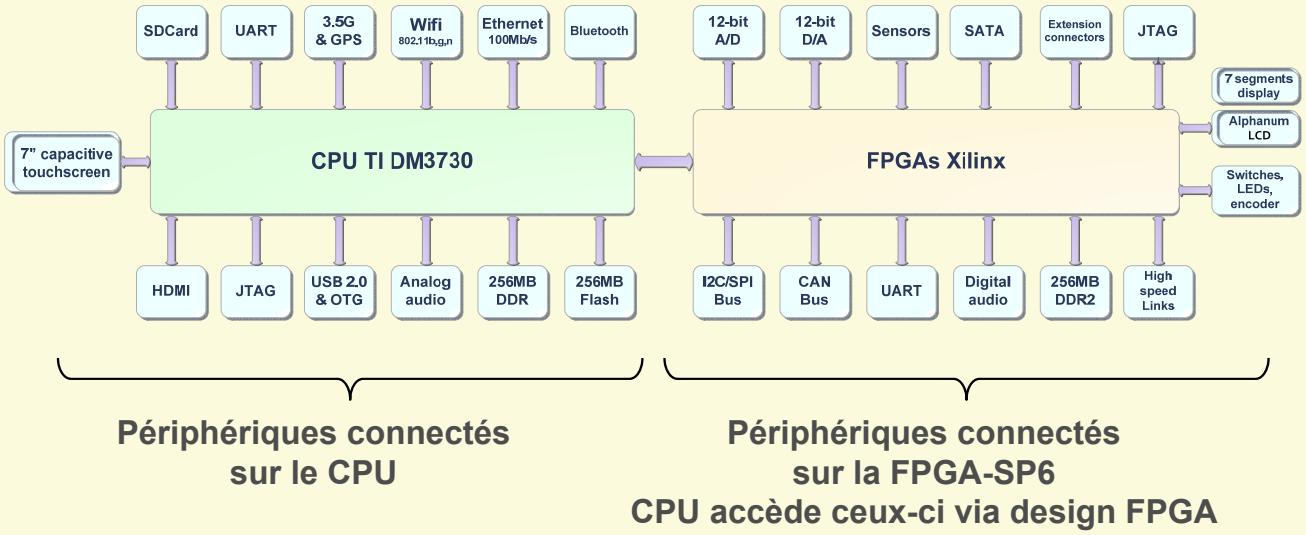
Plateforme REPTAR

- Utilisée pour IFS, ASP et autres …
- Etude/utilisation d'une plateforme embarquée
- Composée de:
  - module DM3730 basé sur un Cortex-A8
  - FPGA Spartan-6
  - un écran tactile 7" (800x480 capacitif)
  - de nombreux périphériques

voir Reptar_Short_Datasheet.pdf

Bloc diagramme REPTAR

- Vue générale de la plateforme REPTAR



Structure DM3730

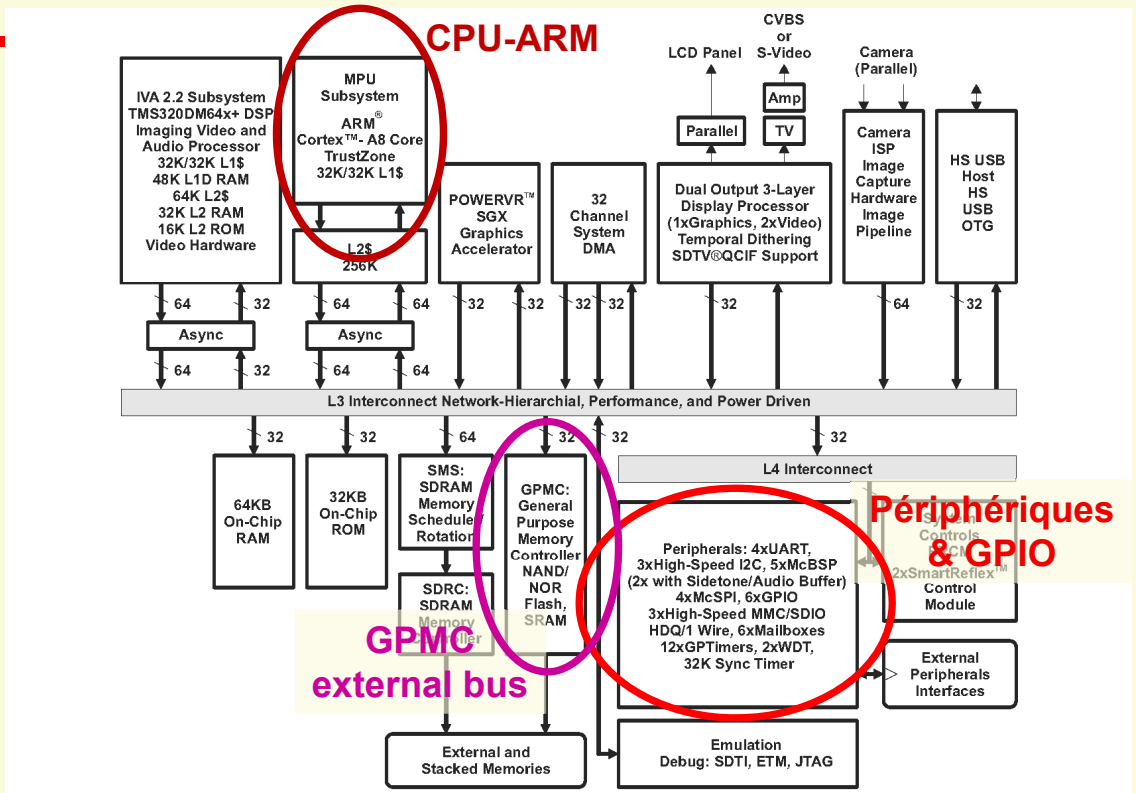
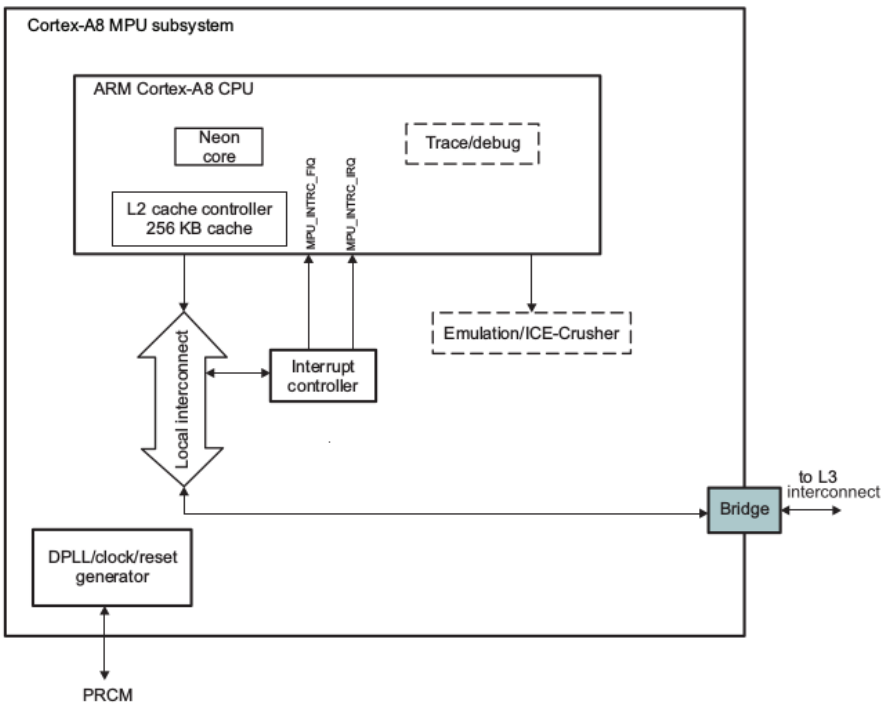


Figure 1-1. DM3730/25 Functional Block Diagram

Structure MPU subsystem

MPU : Microprocessor unit

- ARM Cortex-A8
- Neon (co-processor)
- L2 cache
- Interrupt controller
- Bridge to L3
- Clock generator



DM3730

Plan d'adressage complet du module DM3730

Table 2-1. Global Memory Space Mapping

Quarter	Device Name	Start Address (Hex)	End Address (Hex)	Size	Description
Q0 (1GB)	**Boot space[1] GPMC**			**1MB 1GB or 1GB-1MB**	
	GPMC	0x0000 0000	0x3FFF FFFF	1GB	8/16 Ex[2]/R/W
Q1 (1GB)	**On-chip memory**			**128MB**	**ROM/SRAM address space**
	Boot ROM internal[1]	0x4000 0000	0x4001 3FFF	80KB	Reserved for boot code Not accessible after boot
		0x4001 4000	0x4001 BFFF	32KB	32-bit Ex[2]/R
	Reserved	0x4001 C000	0x400F FFFF	912KB	Reserved
	Reserved	0x4010 0000	0x401F FFFF	1MB	Reserved
	SRAM internal	0x4020 0000	0x4020 FFFF	64KB	32-bit Ex[2]/RW
	Reserved	0x4021 0000	0x4024 FFFF	256KB	Reserved
	Reserved	0x4025 0000	0x47FF FFFF	128,704KB	Reserved
	L4 interconnects			**128MB**	**All system peripherals**
	L4-Core	0x4800 0000	0x48FF FFFF	16MB	See Table 2-3.
	(L4-Wakeup)[3]	(0x4830 0000)	(0x4833 FFFF)	(256KB)	See Table 2-4.
	L4-Per	0x4900 0000	0x490F FFFF	1MB	See Table 2-5.
	Reserved	0x4910 0000	0x4FFF FFFF	111MB	Reserved
	SGX			**64MB**	**Graphic accelerator slave port**
	SGX	0x5000 0000	0x5000 FFFF	64KB	Graphic accelerator slave port
	Reserved	0x5001 0000	0x53FF FFFF	65,472KB	Reserved
	L4 emulation			**64MB**	**Emulation**
	L4-Emu	0x5400 0000	0x547F FFFF	8MB	See Table 2-6.
	Reserved	0x5480 0000	0x57FF FFFF	56MB	Reserved
	Reserved			**64MB**	**Reserved**
	Reserved	0x5800 0000	0x5BFF 0FFF	64MB	Reserved
	IVA2.2 subsystem			**64MB**	**IVA2.2 subsystem**
	IVA2.2 subsystem	0x5C00 0000	0x5EFF FFFF	48MB	IVA2.2 subsystem. See Table 2-8.
	Reserved	0x5F00 0000	0x5FFF FFFF	16MB	Reserved
	Reserved			**128MB**	**Reserved**
	Reserved	0x6000 0000	0x67FF FFFF	128MB	Reserved
	L3 interconnect			**128MB**	**Control registers**
	L3 control registers	0x6800 0000	0x68FF FFFF	16MB	See Table 2-2.
	Reserved	0x6900 0000	0x6BFF FFFF	48MB	Reserved
	SMS registers	0x6C00 0000	0x6CFF FFFF	16MB	Configuration registers SMS address space 2
	SDRC registers	0x6D00 0000	0x6DFF FFFF	16MB	Configuration registers SMS address space 3
	GPMC registers	0x6E00 0000	0x6EFF FFFF	16MB	Configuration registers GPMC address space 1
	Reserved	0x6F00 0000	0x6FFF FFFF	16MB	Reserved
	SDRC/SMS			**256MB**	**SDRC/SMS**
	SDRC/SMS virtual Address space 0	0x7000 0000	0x7FFF FFFF	256MB	SDRC-SMS virtual address space 0
Q2 (1GB)	**SDRC/SMS**			**1GB**	**SDRAM main address space (SMS)**
	CS0 – SDRAM[4]	0x8000 0000	0x9FFF FFFF	512MB	SDRC/SMS
	CS1 – SDRAM[4]	0xA000 0000	0xBFFF FFFF	512MB	SDRC/SMS
Q3 (1GB)	**Reserved**			**512MB**	**Reserved**
	Reserved	0xC000 0000	0xDFFF FFFF	512MB	Reserved for future use
	SDRC/SMS			**512MB**	**SDRC/SMS**
	SDRC/SMS virtual Address space 1	0xE000 0000	0xFFFF FFFF	512MB	SDRC-SMS virtual address space 1

DM3730: GPMC & Periph.

- Vue partielle du plan d'adressage

Table 2-1. Global Memory Space Mapping

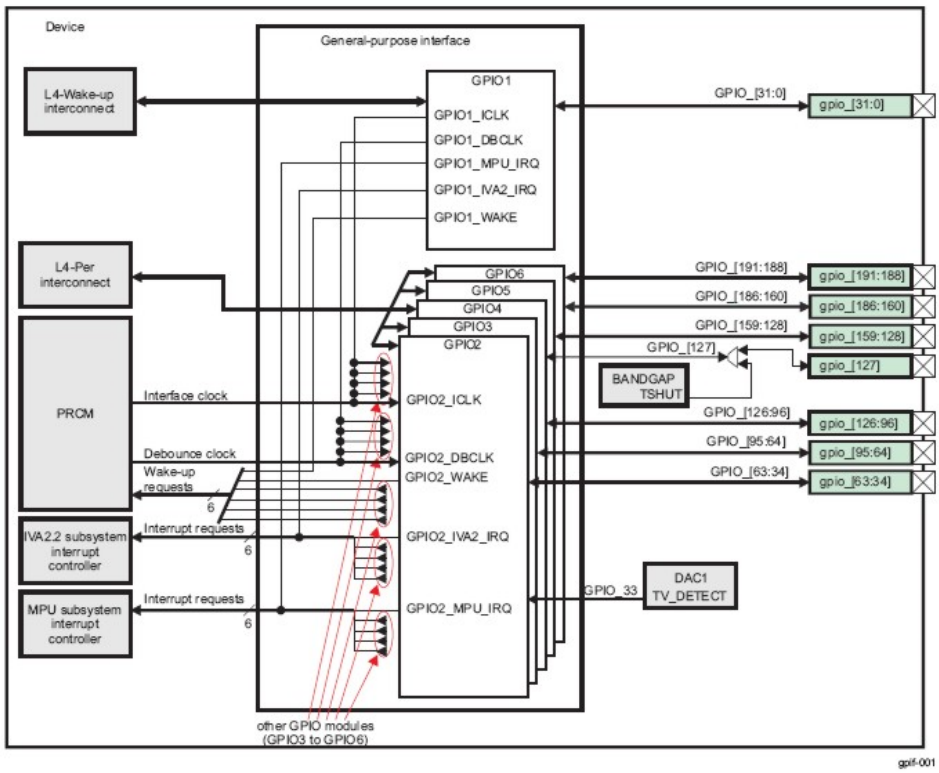
Quarter	Device Name	Start Address (Hex)	End Address (Hex)	Size	Description
Q0 (1GB)	**Boot space[1] GPMC**			**1MB 1GB or 1GB-1MB**	
	GPMC	0x0000 0000	0x3FFF FFFF	1GB	8/16 Ex[2]/R/W
Q1 (1GB)	**On-chip memory**			**128MB**	**ROM/SRAM address space**
	Boot ROM internal[1]	0x4000 0000	0x4001 3FFF	80KB	Reserved for boot code Not accessible after boot
		0x4001 4000	0x4001 BFFF	32KB	32-bit Ex[2]/R
	Reserved	0x4001 C000	0x400F FFFF	912KB	Reserved
	Reserved	0x4010 0000	0x401F FFFF	1MB	Reserved
	SRAM internal	0x4020 0000	0x4020 FFFF	64KB	32-bit Ex[2]/RW
	Reserved	0x4021 0000	0x4024 FFFF	256KB	Reserved
	Reserved	0x4025 0000	0x47FF FFFF	128,704KB	Reserved
	L4 interconnects			**128MB**	**All system peripherals**
	L4-Core	0x4800 0000	0x48FF FFFF	16MB	See Table 2-3.
	(L4-Wakeup)[3]	(0x4830 0000)	(0x4833 FFFF)	(256KB)	See Table 2-4.
	L4-Per	0x4900 0000	0x490F FFFF	1MB	See Table 2-5.

GPMC: Global Memory Controller

Périphériques du DM3730

Structure des groupes GPIO

Figure 25-1. General-Purpose Interface Overview



Structure de l'interface d'un GPIO

25.4 General-Purpose Interface Functional Description

Figure 25-5 shows the general-purpose interface description.

Figure 25-5. General-Purpose Interface Description

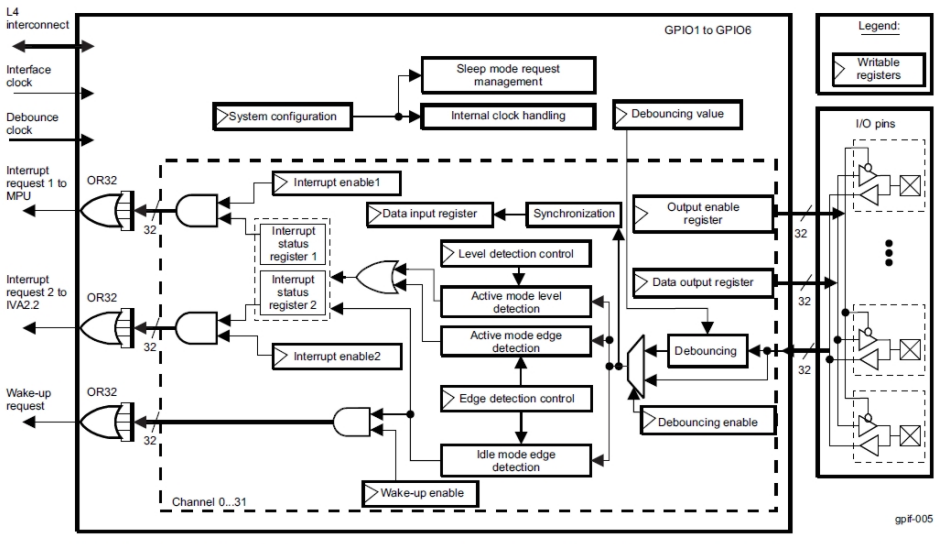


Figure 25-5 details GPIOs in the general-purpose interface block diagram with their configuration registers and their main functional paths:

Périphériques GPIO du DM3730

- Zone L4 core & wake-up

Table 2-3. L4-Core Memory Space Mapping (1)

Device Name	Start Address (Hex)	End Address (Hex)	Size	Description
L4-Core	0x4800 0000	0x48FF FFFF	16MB	
Reserved	0x4800 0000	0x4800 1FFF	8KB	Reserved
System control module (SCM)	0x4800 2000	0x4800 2FFF	4KB	Module
	0x4800 3000	0x4800 3FFF	4KB	L4 interconnect
Clock manager • DPLL	0x4800 4000	0x4800 5FFF	8KB	Module region A
	0x4800 6000	0x4800 67FF	2KB	Module region B

zone pour accéder au GPIO, groupe 1 (Bank 1)

	0x4830 9000	0x4830 9FFF	4	L4 interconnect
Reserved	0x4830 A000	0x4830 FFFF	24	Reserved
GPIO1	0x4831 0000	0x4831 0FFF	4	Module
	0x4831 1000	0x4831 1FFF	4	L4 interconnect
Reserved	0x4831 2000	0x4831 3FFF	8	Reserved

Périphériques GPIO du DM3730

- Zone L4 peripheral

Table 2-5. L4-Peripheral Memory Space Mapping

Device Name	Start Address (Hex)	End Address (Hex)	Size	Description
L4-Per	0x4900 0000	0x490F FFFF	1MB	
L4-Per configuration	0x4900 0000	0x4900 07FF	2KB	AP
	0x4900 0800	0x4900 0FFF	2KB	IP
	0x4900 1000	0x4900 1FFF	4KB	LA

zone pour accéder au GPIO groupes 2 à 6 (Bank 2 to 6)

Reserved	0x4904 4000	0x4904 FFFF	48KB	Reserved
GPIO2	0x4905 0000	0x4905 0FFF	4KB	Module
	0x4905 1000	0x4905 1FFF	4KB	L4 interconnect
GPIO3	0x4905 2000	0x4905 2FFF	4KB	Module
	0x4905 3000	0x4905 3FFF	4KB	L4 interconnect
GPIO4	0x4905 4000	0x4905 4FFF	4KB	Module
	0x4905 5000	0x4905 5FFF	4KB	L4 interconnect
GPIO5	0x4905 6000	0x4905 6FFF	4KB	Module
	0x4905 7000	0x4905 7FFF	4KB	L4 interconnect
GPIO6	0x4905 8000	0x4905 8FFF	4KB	Module
	0x4905 9000	0x4905 9FFF	4KB	L4 interconnect
Reserved	0x4905 A000	0x490F FFFF	664KB	Reserved

Plan d'adressage carte REPTAR

Adresse		DM3730	REPTAR	Description
0x0000 0000	0x000F FFFF	Boot space		Boot space 1MB
0x0010 0000	0x17FF FFFF	GPMC		
0x1800 0000	0x1FFF FFFF		FPGA SP6/SP3	GPMC CS3 (128 MB), asynchr.
0x2000 0000	0x27FF FFFF		FPGA SP6	GPMC CS4 (128 MB), synchr.
0x2800 0000	0x2BFF FFFF			
0x2C00 0000	0x2FFF FFFF		Ethernet	GPMC CS5 (64MB)
0x3000 0000	0x3FFF FFFF	GPMC	Nand Flash	GPMC CS0 (256MB)
0x4000 0000	0x400F FFFF	On-chip		Boot ROM interne
0x4010 0000	0x47FF FFFF	memory		RAM interne
0x4800 0000	0x48FF FFFF	L4-Core		Peripherals & GPIO
0x4900 0000	0x49DF FFFF	L4-Per		Peripherals & GPIO
0x49E0 0000				
	0x67FF FFFF			
0x6800 0000	0x6FFF FFFF	L3 interconnect		
0x7000 0000				
0x7FFF FFFF				
0x8000 0000	0x8FFF FFFF	SDRAM 1GB		SRAM 256 MB
0x9000 0000		controller		
	0xBFFF FFFF			
0xC000 0000				
	0xFFFF FFFF			

Plan adressage GPMC-REPTAR

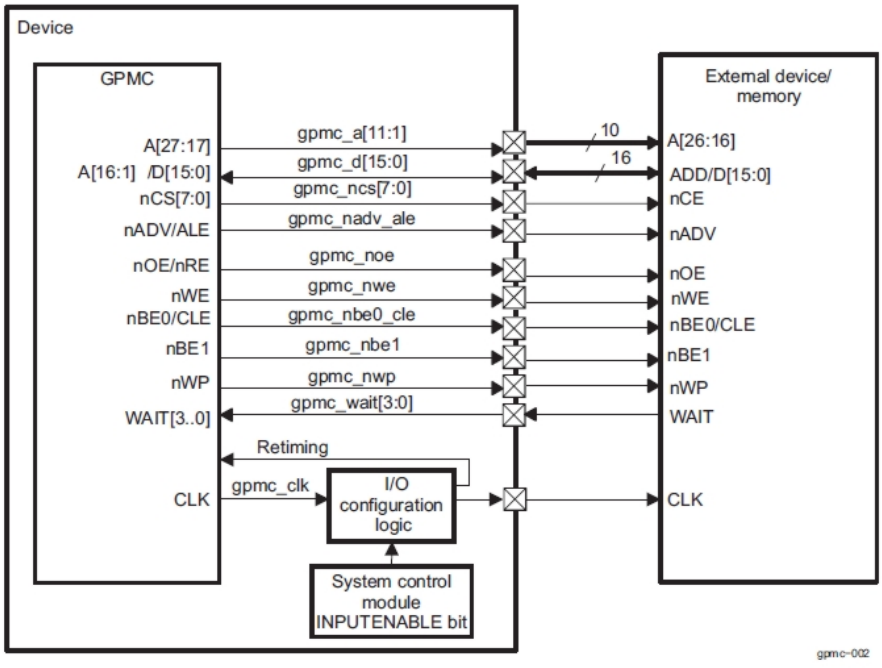
Adresse		DM3730	REPTAR	Description
0x0010 0000	0x17FF FFFF	GPMC		non utilisé
0x1800 0000			FPGA	GPMC CS3 (128 MB),
	0x19FF FFFF		SP6, 32MB	Local bus mode asynchrone
0x1A00 0000			FPGA	
	0x1BFF FFFF		SP3, 32MB	
0x1C00 0000			Inaccessible	
	0x1FFF FFFF		64MB	
0x2000 0000			FPGA SP6	GPMC CS4 (128 MB),
	0x23FF FFFF		SP6 64MB	Local bus mode synchrone
0x2400 0000			Inaccessible	
	0x27FF FFFF		64MB	
0x2800 0000				non utilisé
	0x2BFF FFFF			
0x2C00 0000			Ethernet	GPMC CS5 (64MB)
	0x2FFF FFFF			
0x3000 0000			Nand Flash	GPMC CS0 (256 MB)
	0x3FFF FFFF	GPMC		

General-Purpose Memory Controller (GPMC)

- Contrôleur mémoire à usage général
  - bus d'adresse de 27 bits, dont 16 multiplexés
    - remarque: adresse en word 16 bits !!
  - bus de données de 16 bits multiplexés
  - plage adressable: 128M x 16bits soit 256MB
  - différents protocole: asynchrone, synchrone, …
  - 8 CS configurable dans le 1er quadrant: Q0
    - plage
  - zone du premier quadrant Q0
  - configuration via des registres ….

Signaux du bus du GPMC (local bus)

Figure 10-2. GPMC to 16-Bit Address/Data-Multiplexed Memory



Signaux du bus du GPMC (local bus)

- Lignes d'adresse disponibles sur le local bus du GPMC:
  - The device (GPMC) **does not provide the A0 byte address line** required for random-byte addressable 8-bit-wide device interfacing.
  - An 8-bit device must be connected to D[7:0] / gpmc_d[7:0] data bus of the GPMC (rather than D[15:8] gpmc_d[15:8]). This limits the use of 8-bit-wide device interfacing to byte-alias

Protocole d'accès sur le bus GPMC

- Convention CPU: adressage par byte
- Bus GPMC: bus de data de 16bits
  - ligne d'adresse A0 du CPU pas transmise
  - deux signaux indiquent les bytes valides pour le transfert en cours :
    - BE0 pour les bytes pairs, correspondant à A0 = '0'
    - BE1 pour les bytes impairs, correspondant à A0 = '1'
    - **BE** pour **B**yte **E**nable

Plan d'adressage des FPGAs

Adresse		DM3730	CS3	CS4	FPGA	Mode	Size	Use	Description
….		GPMC	'0'	'0'					
	0x17FF_FFFF	GPMC	'0'	'0'					
0x1800_0000	0x180F_FFFF	GPMC	'1'	'0'	SP6		1MB	Std	Standard interface
0x1810_0000			'1'			Asynchr.	15MB	Std	Reserved
	0x18FF_FFFF		'1'		SP6			Std	
0x1900_0000	0x193F_FFFF		'1'		SP6		4MB	User	User interface (labs & demos)
0x1940_0000			'1'			Asynchr.	12MB	User	Reserved
	0x19FF_FFFF	GPMC	'1'	'0'	SP6			User	
0x1A00 0000		GPMC	'1'	'0'	SP3		1MB	Std	Standard interface
			'1'			Asynchr.	31MB	Std	Reserved
	0x1BFF_FFFF		'1'		SP3			Std	
0x1C00_0000			'1'						
			'1'				64MB		Inacessible
	0x1FFF_FFFF		'1'	'0'					
0x2000_0000			'0'	'1'	SP6				Local bus mode synchrone
				'1'		Synchr.			for access to DDR2 or
	0x1BFF_FFFF			'1'	SP6				special user interface
0x1C00_0000				'1'					
				'1'			64MB		Inacessible
	0x27FF_FFFF	GPMC	'0'	'1'					
0x2800_0000									

Plan adressage GPMC-FPGA SP6 et SP3

Adresse		DM3730	CS3	CS4	FPGA	Mode	Size	Use	Description
	0x17FF FFFF	GPMC	'0'	'0'					
0x1800 0000	0x180F_FFFF	GPMC	'1'	'0'	SP6		1MB	Std	Standard interface
0x1810_0000	0x182F_FFFF		'1'				2MB	Std	Unused
0x1830_0000	0x183F_FFFF		'1'			Asynchr.	1MB	Std	Peripherals descriptors table
0x1840_0000	0x187F_FFFF		'1'				4MB	Std	REDS - internal designs
0x1880_0000	0x18BF_FFFF		'1'				4MB	Std	REDS - internal designs
0x18C0_0000	0x18FF_FFFF		'1'		"		4MB	Std	Unused/reseverd
0x1900_0000	0x193F_FFFF		'1'				4MB	User	REDS - labs and demos
0x1940_0000	0x197F_FFFF		'1'			Asynchr.	4MB	User	REDS - labs and demos
0x1980_0000	0x19BF_FFFF		'1'				4MB	User	REDS - external projects
0x19C0_0000	0x19FF FFFF	GPMC	'1'	'0'	SP6		4MB	User	EXT USER - free to use
0x1A00 0000		GPMC	'1'	'0'	SP3			Std	Standard interface
			'1'			Asynchr.	32MB	Std	
	0x1BFF_FFFF		'1'		SP3			Std	
0x1C00_0000			'1'						

Plan d'adressage des FPGAs

- La carte REPTAR dispose de 2 FPGAs
  - FPGA Spartan 6
    - Utilisée avec un projet Logisim
    - Conception et réalisation d'interfaces dans la zone d'adressage "user interface" soit : 0x1900_0000 - 0x193F_FFFF
    - Zone d'adressage "standard" n'est pas utilisée sauf pour les 2 registres avec les versions.
      - plage d'adresse standard: 0x1800_0000 - 0x18FF_FFFF
      - registres implémentés:
        0x1800_0000: HW-version, ID-FPGA, ID-design-FPGA
      - 0x1800_0002: ID-sub-design, version-number

Plan d'adressage des FPGAs

- La carte REPTAR dispose de 2 FPGAs
  - FPGA Spartan 3
    - Utilisation du design standard (chargé au boot)
    - Utilisation des I/O simples
    - Voir : Spartan3_registers_ifs.xlsx