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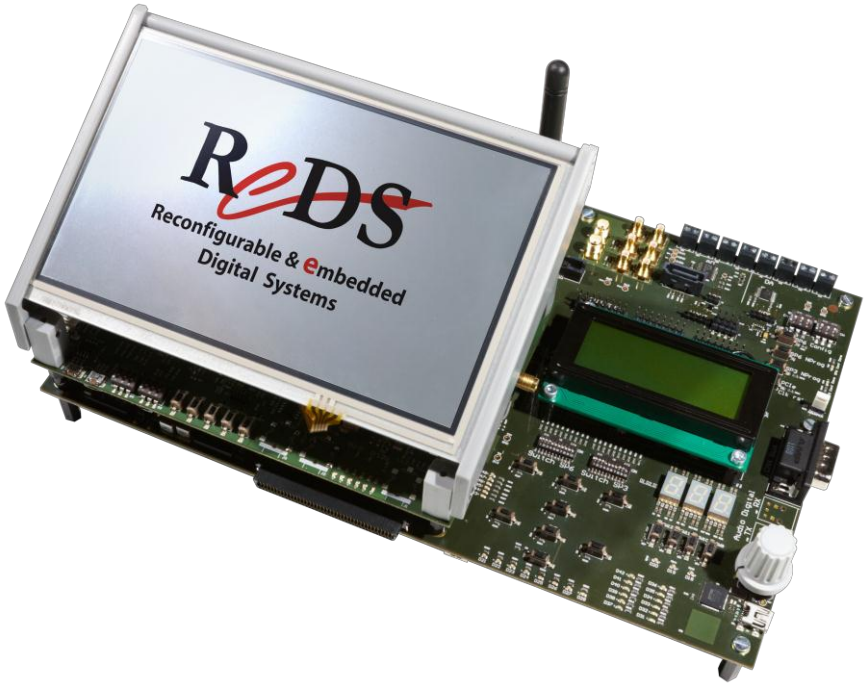
ReDS
Reconfigurable & embedded
Digital Systems

REPTAR Development Board

Reference Manual



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1. INTRODUCTION

REPTAR is a modular extensible platform for teaching and R&D in the HES-SO and beyond...

- **TEACHING**

REPTAR is a Universal board for workshops, courses in computer architecture and embedded processor-based systems. The REPTAR platform allows federating various laboratories by providing a common platform.

REPTAR combines an OMAP processor type based on DaVinci DM3730 from Texas Instrument (which itself consists of a core-A8 ARM and a DSP) with a programmable component (FPGA) Xilinx Spartan 6. The platform also includes a large number of control devices, display and communication. Modular in design, it offers many possibilities for expansion.

From a programming perspective, the workshops can be done in different ways:

- Development at the application level or in the processor core with OS or RTOS without intervention in FPGA.
- Development without low-level OS and without intervention in FPGA
- Application Development in the FPGA without CPU usage
- Mix development of processor and FPGA code

- **RESEARCH AND DEVELOPPMENT**

REPTAR is a development platform suitable for many research projects, making it unnecessary, at least initially, the realization of a project dedicated board.

2. GENERAL DESCRIPTION

REPTAR is a board that offers a unique opportunity to customize your development environment via many expansion connectors, I/O and daughter cards.

The REPTAR board is made of two boards:

- The CPU and the FPGA board

The FPGA board is considered as the mainboard of the REPTAR system. All the power supplies are located on this board. The CPU board is then considered as a daughter card for the system itself. Nevertheless, it is possible to use it separately by connecting it to an optional power supply board[1].

2.1 BLOC DIAGRAM

The figure below depicts a functional block diagram of the REPTAR board.

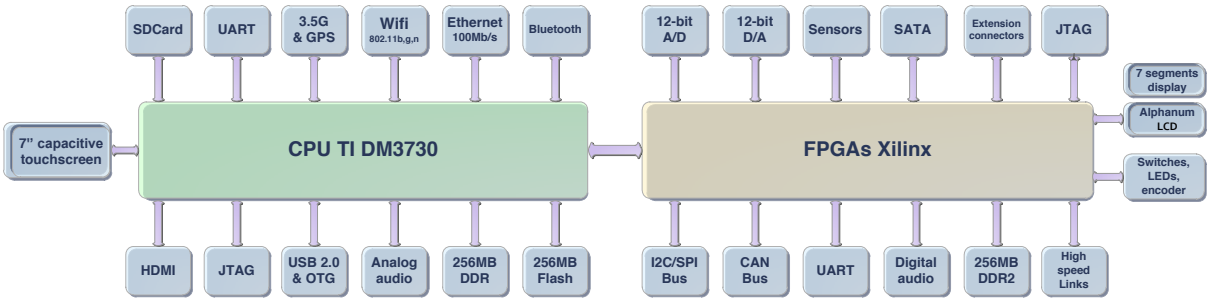


Figure 1 - REPTAR bloc diagram

This illustration shows the complexity of the REPTAR system. Not less than 28 peripherals are present on it. These peripherals will be described in the next chapters.

[1] Available on demand

2.2 BOARD COMPONENTS BLOCKS

- **Processor module** DM3730 based on Cortex-A8 (compatible with OMAP 3)
  - 1 GHz operating frequency
  - 256MB of DDR memory
  - 256MB of flash memory
  - SD-card interface
  - Display interface for TFT / HDMI output
  - UART / I2C / SPI interfaces
  - 100Mbit Ethernet interface
  - 16 bit linear audio stereo DAC / ADC
  - MIC and Line In & Out
  - USB 2.0 Host and OTG interfaces
  - Capacitive touch screen interface

- **FPGA** Xilinx Spartan6
  - XC6SLX150TFGG900-3
  - 147'443 Logic elements
  - 184'304 Flip-flop
  - 1'335Kbit of distributed RAM
  - 4'824Kbit of Blocks RAM
  - 4 MCB
  - 8 Transceivers (GTP) @ 3GHz

- **Configuration subsystem**
  - Xilinx Spartan3 AN XC3S200AN-5FTG256C
    - Bitstream stored in internal flash
    - Used for Spartan6 download
  - Xilinx PlatformFlash XCF32P
    - Store up to 4 compressed bitstream for Spartan6

- **Display interfaces**
  - EDT 7" display with capacitive touch screen
    - 800 x 480
    - I2C for touch
  - LCD display
    - 4 x 20 lines
  - 7-segments

- **Memory subsystem**
  - External DDR2 SDRAM device (on Spartan6 FPGA)
    - 256MB
    - @ 800 MHz
  - Parallel Flash memory (on CPU module)
    - 256MB
  - DDR SDRAM device (on CPU module)
    - 256MB
    - @ 400 MHz
  - SD-card interface (on CPU module)

- **Clock management system**
  - One 150MHz (for SATA subsystem)
  - One 125MHz (for PCIe subsystem)
  - One 100MHz for Spartan6 internal logic
  - One 100MHz for Spartan3AN internal logic
  - One slow clock at 25MHz for both Spartan6 and Spartan3AN internal logic
  - The Spartan6 FPGA distributes the following clocks from its internal PLLs :
    - External DDR2 memory
    - PCIe interface
    - SATA interface

- **Wired and Wireless communication subsystem**
  - 100Mbit Ethernet feature (on CPU module)
  - WIFI & Bluetooth Module
    - IEEE 802.11 b/g/n compatible
    - BT 2.1 compatible

  - GPS & GSM Module
    - PCI Express mini card full size module
    - HSPA, UMTS, EDGE, GPRS and SMS capabilities
    - Assisted-GPS

- **Expansion connectors**
  - Two FMC LPC connectors
    - Provides each 34 differential lines or 58 single-ended signals
    - It also provides one serial high speed differential pair, clocks, a JTAG Interface and an I2C interface
  - One DHB DDK connector
    - Provides 78 GPIOs signals from Spartan6 FPGA

- **General User Interface**
  All these components are located either on the CPU or on the FPGA board and provide an easier way to debug the user designs.
  - Leds and buttons
  - Switches
  - Headers

- **Serial interfaces**
  All these interfaces are connecting the CPU, FPGA and various sensors together.
  - I2C
  - SPI
  - CAN

- **Audio subsystem**
  - 16 bit audio stereo analog
    - One mini jack line In
    - One mini jack line Out (pre-amp)
    - One mini jack Microphone
  - Digital audio
    - One Toslink receiver
    - One Toslink transmitter

- **USB subsystem**
  - 6 Host connectors
  - 1 OTG connector
  - 1 USB-UART connection direct to FPGA
  - 1 USB-UART connection direct to CPU for debugging

- **High speed links**
  - Three SMB connectors provide access to the high speed transceivers of the Spartan6
    - One differential input
    - One differential output
    - One reference input clock
  - A PCI Express connection between Spartan6 and CPU board [2]
    - Provides 2 lanes
    - Internal or external reference clock
  - A SATA 1 link between Spartan6 and CPU board [2,3]
  - An external SATA 1 connector from Spartan6 [3]

[2] Not available on CPU board revision 1.0
[3] Require a third party vendor IP – not provided by the REDS

- **Sensors and actuators**
  - Temperature sensor
  - Light sensor
  - Buzzer
  - Incremental encoder

- **AD & DA converters**
  - 12-bit ADC
    - Quad channels
    - SPI interface
    - Single 3V-to-5V power supply
  - 12-bit DAC
    - Quad channels
    - 1 MHz sample rate
    - SPI interface
    - Analog Supply Range: 2.7 to 5.25V
    - Digital Supply Range: 1.7 to 5.25 V

3. BOARD COMPONENTS AND INTERFACES

3.1 BOARD OVERVIEW

Chapter 3 provides operational and connectivity details for the major components and interfaces of the board and is divided into the following blocks:

- Main devices
  - DM3730 CPU module
  - Spartan 6
  - Spartan 3AN
- Display
  - TFT 7" with capacitive touch screen
- Memory
  - DDR/DDR2
  - Flash
  - SD-card
- Communications
  - USB interface
  - High-speed serial interface
  - Expansion connectors
- General user interfaces
  - Jumpers
  - Connectors
  - Buttons
- Sensors and Actuators
- AD & DA
- Audio
  - Analogic
  - Digital
- Clocking circuitry
- Configuration circuitry
- Debugging
  - Connectors
  - JTAG
  - UART
- Power supply

3.1.1 FPGA board overview

The picture below depicts where are located all the different functionalities described in the following chapters.

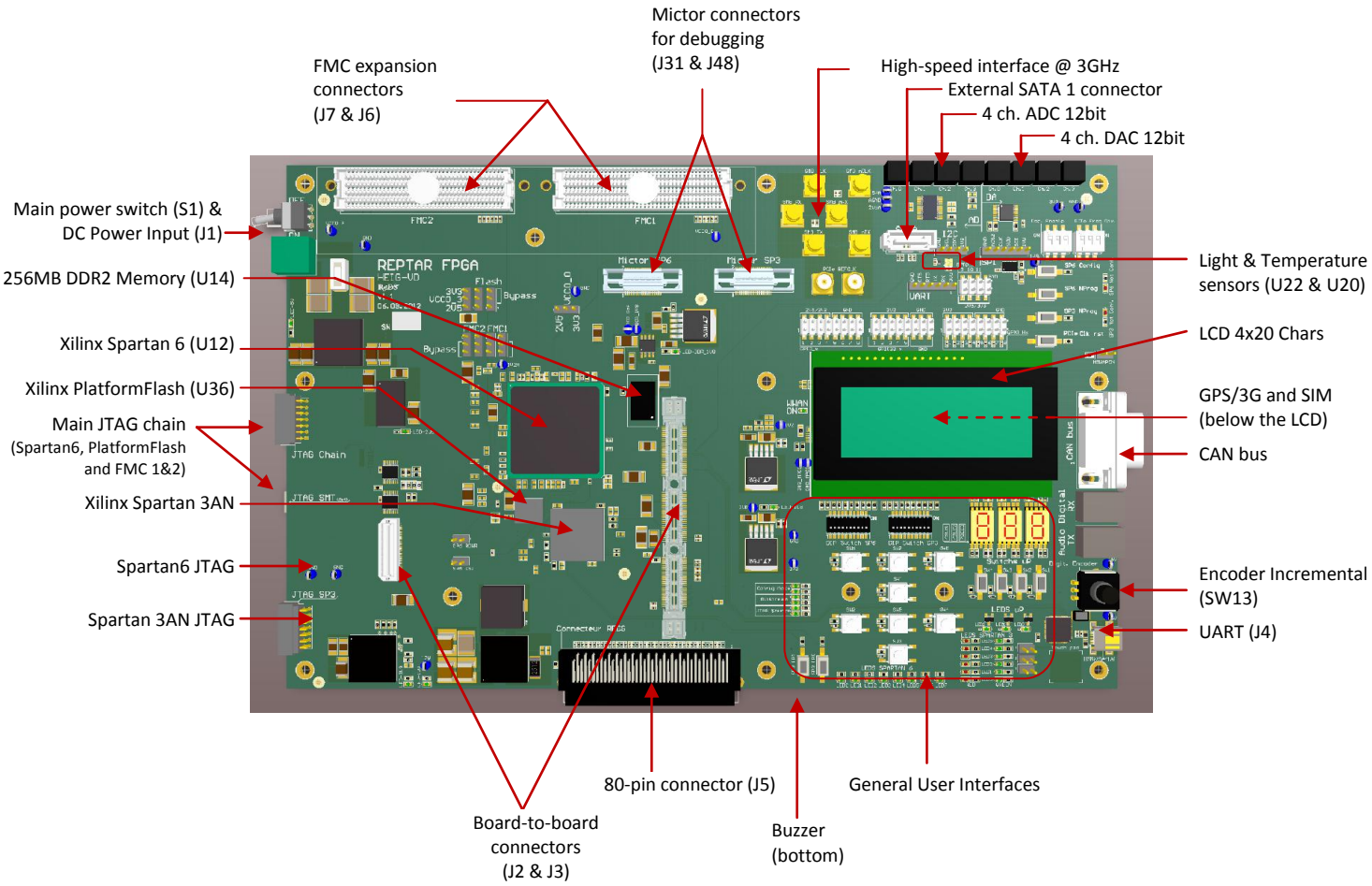


Figure 2 - FPGA Board details

3.1.2 CPU board overview

The picture below depicts where are located all the different functionalities described in the following chapters.

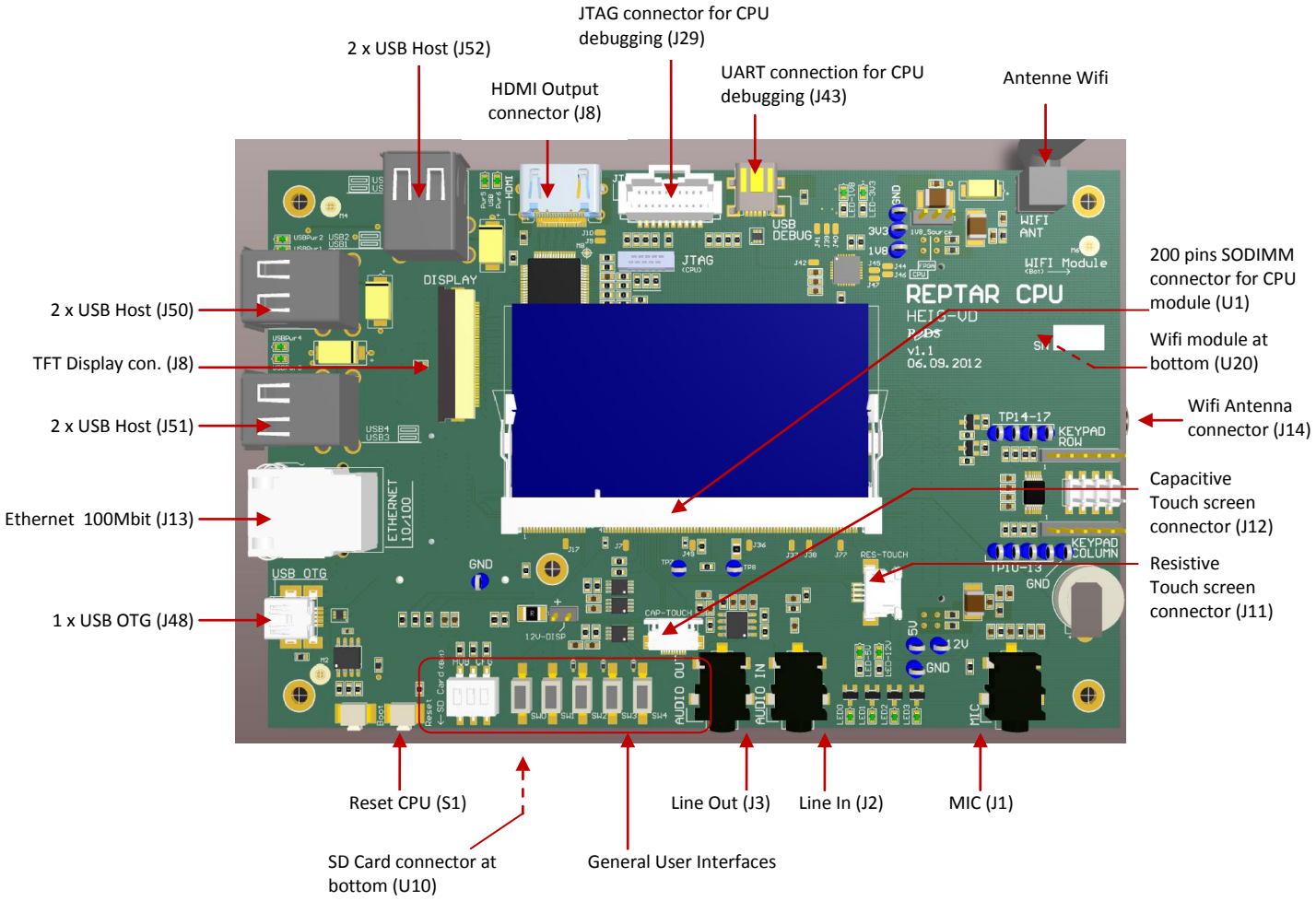


Figure 3 - CPU Board details

3.2 COMPONENTS AND FUNCTIONALITIES

This table describes the main components and their functionalities.

Type	Components / Interfaces	Board Reference	Description	Board Location
Main devices				
FPGA	Xilinx Spartan6 XC6SLX150TFGG900-3	U12	Provides computation power and access to peripherals of the board. Linked to the CPU local bus	FPGA *(fig.2)*
FPGA	Xilinx Spartan 3AN XC3S200AN-5FTG256C	U29	Used to configure the Spartan6 from either the CPU or the on-board PlatformFlash. Linked to the CPU local bus	FPGA *(fig.2)*
Processor	Module Variscite VAR-SOM-OM37	U1	Package 200 pins SODIMM. Based on a TI DM3730 (Cortex A8). Linked to all the FPGAs through its local bus.	CPU *(fig.3)*
Display				
Display	EDT ETM070001ADH6	---	7" Capacitive touch screen. 800 x 480 pixels with white leds for the backlight. *(Possibility to use a resistive touch screen in replacement of the capacitive one)*	CPU
HDMI Out	·HDMI connector ·TI PanelBus Transmitter	J8 U6	·Allow to connect an HD TV in parallel of the 7" LCD display ·Convert the RGB bus of the CPU into a DVI compliant interface.	CPU *(fig.3)*
Display	LCD alpha-numeric	DS1	Provide 4x20 characters. Driven by the Spartan6.	FPGA *(fig.2)*
Memory				
DDR sdram	256MB	Module Variscite	Run @ 400MHz. Only accessible by the processor.	CPU
Flash	256MB	Module Variscite	Only accessible by the processor. Used to store the processor code and FPGA bitstreams.	CPU
SDCard	Molex Secure Digital connector	U10	Provide an alternate storage memory for the processor code (OS, File system …). Accessible at the boot of the CPU.	CPU *(fig.3)*
DDR2 sdram	Micron 16MBx16x8banks MT47H128M16RT-25E:C	U14	Run @ 800MHz. Only accessible by Spartan6. Provide a fast and large external storage memory.	FPGA *(fig.2)*
Communications				
I/O	·3x double USB Host type A ·SMSC USB2517 USB HUB	J50,51,52 U14	·These connectors are linked to the High speed USB 2.0 controller of the CPU module through an on-board USB HUB from SMSC. This HUB offers 7 high-speed ports. ·They provide access to various peripherals (mouse, keyboard, webcam …).	CPU *(fig.3)*

Type	Components / Interfaces	Board Reference	Description	Board Location
I/O	1x mini USB OTG	J48	Directly connected to the USB 2.0 OTG controller of the CPU module.	CPU *(fig.3)*
I/O	Ethernet 100Mb	J13	The Ethernet functionality is natively supported by CPU module. Only the connector is located on the CPU board.	CPU *(fig.3)*
Wifi / Bluetooth	·LS Research Tiwi-R2 module ·SMA connector	U20 J14	·The Tiwi module is offering Wifi and Bluetooth functionalities. It supports 802.11 b/g/n speed and BT 2.1. It is directly connected to the CPU module. ·An SMA connector provides antenna connection for both Wifi and Bluetooth communications.	CPU *(fig.3)*
3G / GPS	·Ericsson F5321GW module ·SIM card con.	J10 P2	This module provides access to 3.5G protocols and to a GPS system. This is a mini PCI Express form factor module. It is connected to the HUB U14. The SIM card is directly managed by the Ericsson module itself.	FPGA *(fig.2)*
High-speed links	Spartan6 transceivers	P3 – P8	Provides 3GHz links from Spartan6 transceivers through differential pairs connected to SMB connectors.	FPGA *(fig.2)*
PCIe links	Spartan6 transceivers	---	Provides two PCI Express lanes between the Spartan6 and the CPU board. PCI reference clock is coming from an on-board reference oscillator or could be driven directly from the CPU board. *(This functionality is not available on the current CPU board.)*	FPGA - CPU
SATA links	Spartan6 transceivers	J32	Provides one SATA 1 connection between the Spartan6 and the CPU board. *(This functionality is not available on the current CPU board)* In addition, a second link is available through an external SATA connector (J32). *(This connection is third vendor IP dependent and not provided by the REDS.)*	FPGA - CPU *(fig.2)*
Expansion	Samtec FMC LPC	J6, J7	Provides 34 differential lines or 58 single-ended signals per FMC connectors. They are linked directly to the Spartan6.	FPGA *(fig.2)*
Expansion	DDK DHB 80 pin	J5	Provides 78 GPIOs (2 GND). Mainly used to connect to REDS proprietary boards	FPGA *(fig.2)*
General user interfaces				
User button	Spartan3AN User Button	SW13, SW14	Provides user dedicated buttons to the Spartan3AN.	FPGA *(fig.4)*
Jumpers	FTDI Jumper eeprom	W11, W12, W13	Disconnect Eeprom from FTDI chip U8 when removed.	FPGA[4] *(fig.4)*
Connector	I2C connector	W2	Provide access to the on-board I2C bus.	FPGA *(fig.5)*

[4] Only available on version 1.0 of the Reptar board

Type	Components / Interfaces	Board Reference	Description	Board Location
Connector	SPI connector	W3	Provide access to the on-board SPI bus.	FPGA *(fig.5)*
Connector	UART connector	W6	Provide access to the on-board UART bus.	FPGA *(fig.5)*
Connector	CAN connection	J45, U27	Provide a compliant CAN bus connection with the Spartan6.	FPGA *(fig.2)*
Switch	Spartan6 user switch	S4	Provides a user dedicated 10 positions switch to the Spartan6.	FPGA *(fig.4)*
Buttons	Spartan6 user	SW1 to SW8	Provides 8x user dedicated buttons to the Spartan6.	FPGA[5] *(fig.4)*
Leds	Spartan6 user leds	D21 to D28	Provides 8x user dedicated leds from the Spartan6.	FPGA[5] *(fig.4)*
Buttons	CPU user buttons	SW9 to SW12	Provides 4x user dedicated buttons to the CPU	FPGA[5] *(fig.4)*
Leds	CPU user leds	D18 to D20	Provides 3x user dedicated leds from the CPU	FPGA[5] *(fig.4)*
Buttons	CPU user buttons	SW0 to SW4	Provides 5x user dedicated buttons to the CPU	CPU[5] *(fig.7)*
Leds	CPU user leds	LED0 to 3	Provides 3x user dedicated leds from the CPU	CPU[5] *(fig.7)*
Sensors and Actuators				
Sensor	Temperature	U20	Provide temperature (I2C link)	FPGA *(fig.5)*
Sensor	Light	U22	Provide luminosity (I2C link)	FPGA *(fig.5)*
Sensor	Accelerometer	U21	Provide accelerometer measure (SPI link)	FPGA *(fig.5)*
Button	Incremental Encoder	SW15	---	FPGA *(fig.4)*
Buzzer	TDK Magnetic buzzer	U28	---	FPGA *(fig.2)*
AD & DA				
ADC	Analog Device ADS7950	U25, J33, J34, J35, J36	12bit, 4 channels analog-to-digital converter. It is connected to 4x two pins screw terminals.	FPGA *(fig.5)*
DAC	Analog Device AD7398	U26, J41, J42, J43, J44	12bit, 4 channels digital-to-analog converter. It is connected to 4x two pins screw terminals.	FPGA *(fig.5)*
Audio				
Digital	Toshiba Toslink	J31, J40	Provide I/O optical audio links to the Spartan6	FPGA *(fig.4)*
Analog Line IN	1x Jack connector	J2	Audio IN link to the CPU.	CPU *(fig.3)*
Preamp. Line OUT	1x Jack connector	J3	Audio OUT from the CPU.	CPU *(fig.3)*
MIC Line	1x Jack connector	J1	MIC Line to the CPU.	CPU *(fig.3)*

[5] Partially available on version 0.1 / Fully available on version 1.0

Type	Components / Interfaces	Board Reference	Description	Board Location
Clocking Circuitry				
100MHz	Main Spartan6 oscillator	Y3	Used to clock internal logic of the Spartan6. It is used to drive the FPGA internal PLLs.	FPGA
100MHz	Main Spartan3AN oscillator	Y5	Used to clock internal logic of the Spartan3AN.	FPGA
25MHz	Common oscillator to Spartan6 and Spartan3A	Y2	Optional slow clock for both FPGAs.	FPGA
125MHz	Dedicated PCIe oscillator	U23	Provide standard clock for the dedicated transceiver PLL used for the PCI Express interface.	FPGA
150MHz	Dedicated SATA oscillator	Y4	Provide standard clock for the dedicated transceiver PLL used for the SATA interface.	FPGA
Configuration circuitry				
Configuration	Xilinx XCF32P PlatformFlash	U36	Used to store up to 4 compressed bit-streams for the Spartan6. Could be used in Slave or Master modes. Programmable through the main JTAG chain.	FPGA *(fig.2)*
Mode switch	Spartan3AN modes selector	S7	Bit 7 to 9 select the configuration mode of the Spartan3AN. Others are user dedicated.	FPGA *(fig.4)*
Button	Spartan6 Reset	S9	Used to reset the Spartan6.	FPGA *(fig.5)*
LED	Spartan6 ConfDone	D30	If on, the Spartan6 is not configured.	FPGA *(fig.5)*
Button	Spartan3AN Reset	S8	Used to reset the Spartan3AN bitstream.	FPGA *(fig.5)*
LED	Spartan3AN ConfDone	D49	If on, the Spartan3AN is not configured.	FPGA *(fig.5)*
Jumper	Spartan6 CSI	W17	Used to disconnect Chip Select functionality (for readback feature) when removed.	FPGA[4]
Jumper	Spartan6 RDWR	W16	Used to disconnect readback functionality when removed.	FPGA[4]
Jumper	Spartan6 VCCO_0 HSWAPEN	P1	Unable HSWAPEN functionality for Spartan6 when removed.	FPGA *(fig.5)*
Jumpers	JTAG chain selector	W7, W8, W9, W10, W14, W15	Taken by two, they allow bypassing FMC2 or FMC1 or PlatformFlash respectively, when in position 2-3.	FPGA[4] *(fig.6)*
JTAG Mux	JTAG source selection	U30, U32	Allow to choose between the JTAG 14 pins connector and the Digilent USB JTAG emulator as the source of the main JTAG chain. This mux is driven by the Spartan3AN.	FPGA *(fig.2)*

Type	Components / Interfaces	Board Reference	Description	Board Location
Debug				
Headers	2x 16 pins headers	J38, J39	Provides debug means for the Spartan6.	FPGA *(fig.5)*
Headers	1x 16 pins headers	J8	Provides debug means for the Spartan6.	FPGA *(fig.5)*
Headers	1x 8 pins headers	W1	Provides debug means for the Spartan6.	FPGA *(fig.5)*
Mictor	1x 38 pins Mictor	J31	Provides debug means for the Spartan6.	FPGA *(fig.2)*
Mictor	1x 38 pins Mictor	J48	Provides debug means for the Spartan3AN.	FPGA *(fig.2)*
Console	·1x CP2103 UART to USB interface ·1x Mini-USB connector	U11, J43	Linux console access via a Mini-USB connector.	CPU *(fig.7 & 3)*
JTAG	1x JTAG TI connector	J29	Provides debug means for the CPU.	CPU *(fig.3)*
Headers	1x 8 pins header	W1	Provides debug means for the CPU.	CPU *(fig.7)*
Power supply				
LED	Power LED	D51, D50, D53, D54, D52, D55	When on, indicated good power state for 5V, 2V5, 3V3, 12V, 1V8 and DDR2_1V8	FPGA[4] (on board)
Jumper	Spartan6 VCCO_0 power selector	W4	Allow to power Spartan6 bank 0 from 2V5 or 3V3.	FPGA *(fig.6)*
Jumper	Spartan6 VCCO_3 power selector	W5	Allow to power Spartan6 bank 3 from 2V5 or 3V3.	FPGA[4] *(fig.6)*
LED	Power LED	D10, D12, D13, D20	When on, indicated good power state for 1V8, 3V3, 5V and 12V	CPU *(on board)*
Jumper	CPU VIO source selector	W2	Choose VIO 1V8 source from FPGA board or COM Module internal regulator	CPU *(fig.7)*
Power RTC	CR1225	X1	3V battery for RTC	CPU

Table 1 - Components & Functionalities details

3.3 DETAILS DRAWINGS

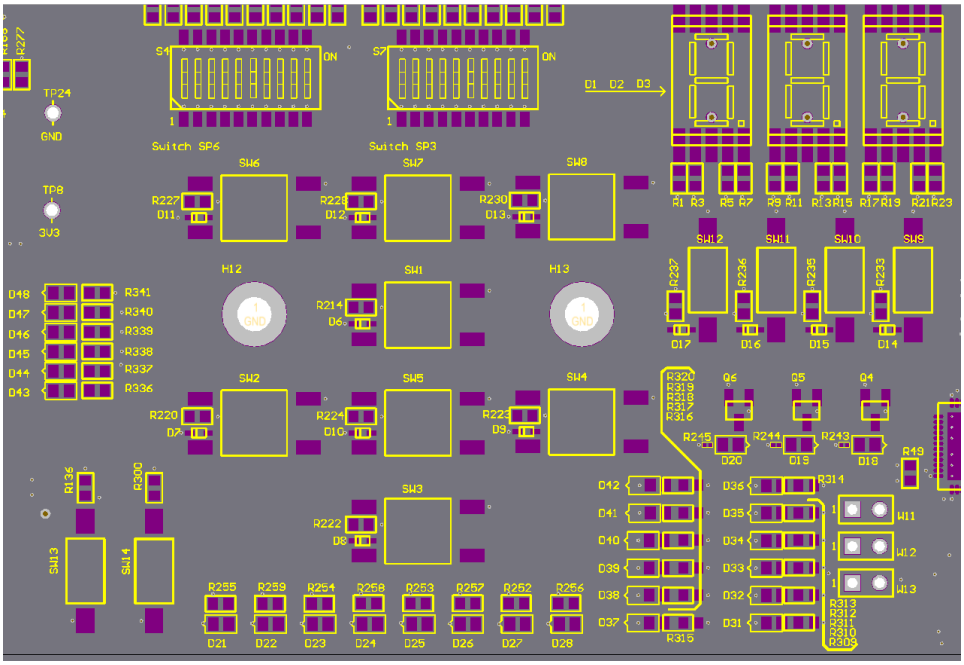


Figure 4- FPGA General User Interfaces

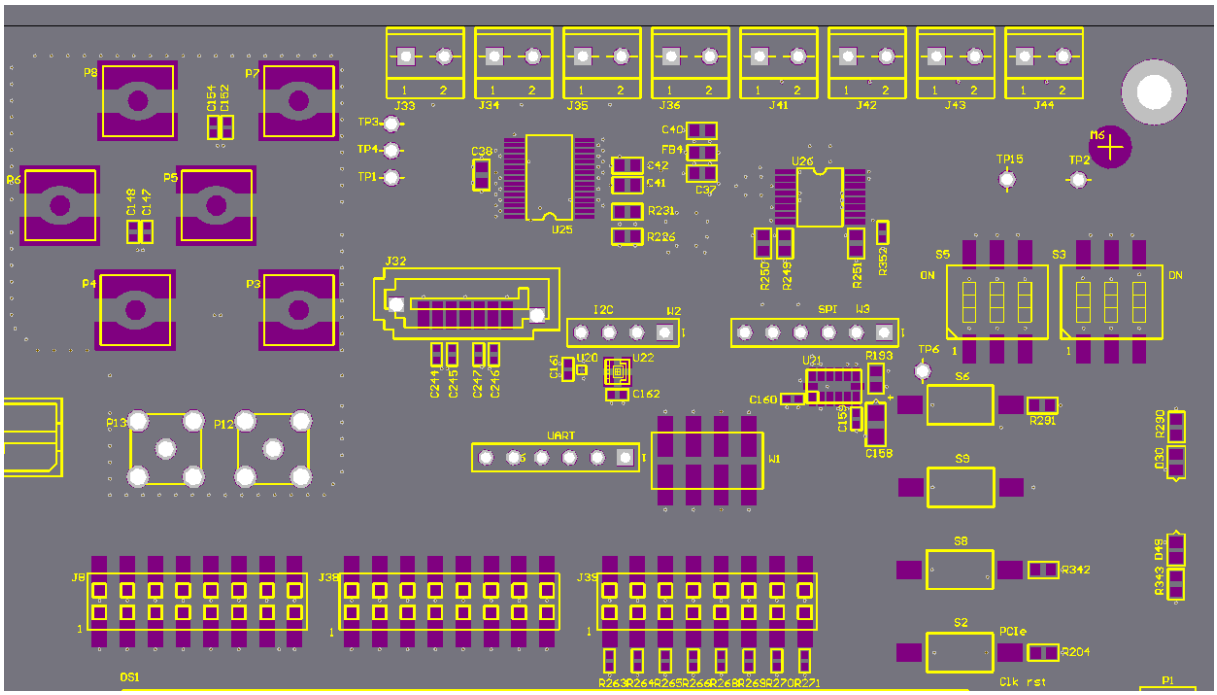


Figure 5 – FPGA Config & Debug switches

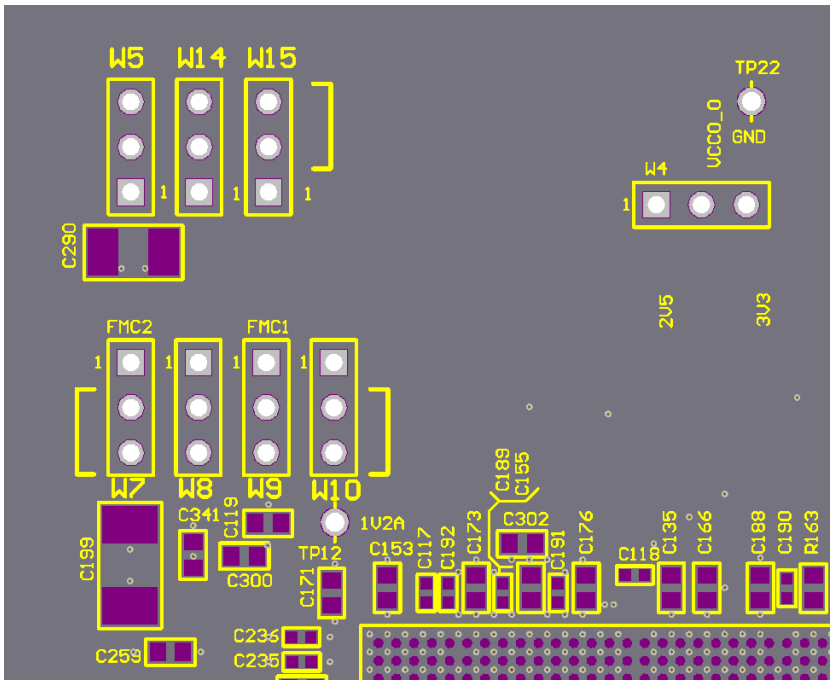


Figure 6 - FPGA Jumpers

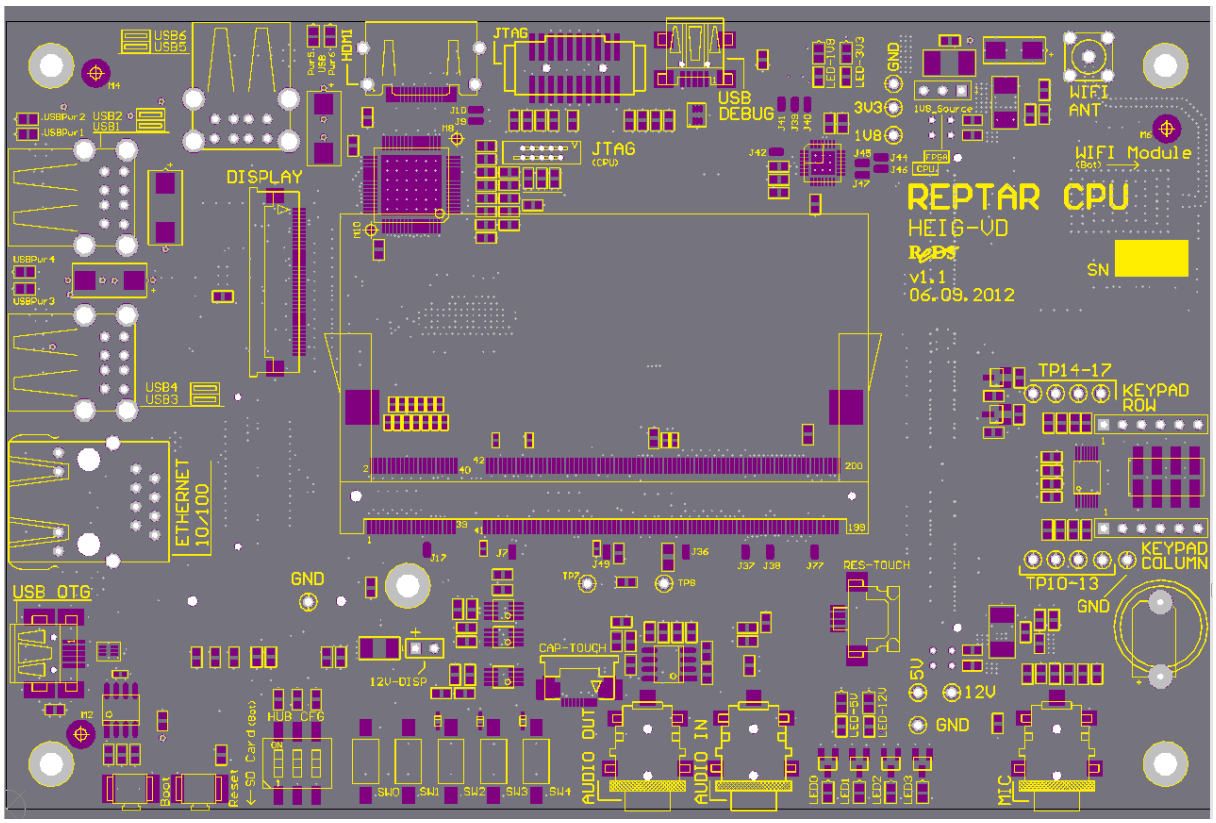


Figure 7 - CPU Label References

3.4 USB INTERFACE

The USB sub-system of the REPTAR board is located onto the CPU board.
The CPU module from Variscite provides two USB 2.0 high-speed controllers. One is a HOST controller and the other is an OTG controller.

The OTG is directly linked to a mini OTG connector, whereas the HOST is attached to a USB HUB 7 ports.

- 6 ports are directly linked to double USB A connectors.
- The remaining port is used to connect, through the BTB[6] connectors, the 3G/GPS module located on the FPGA board.

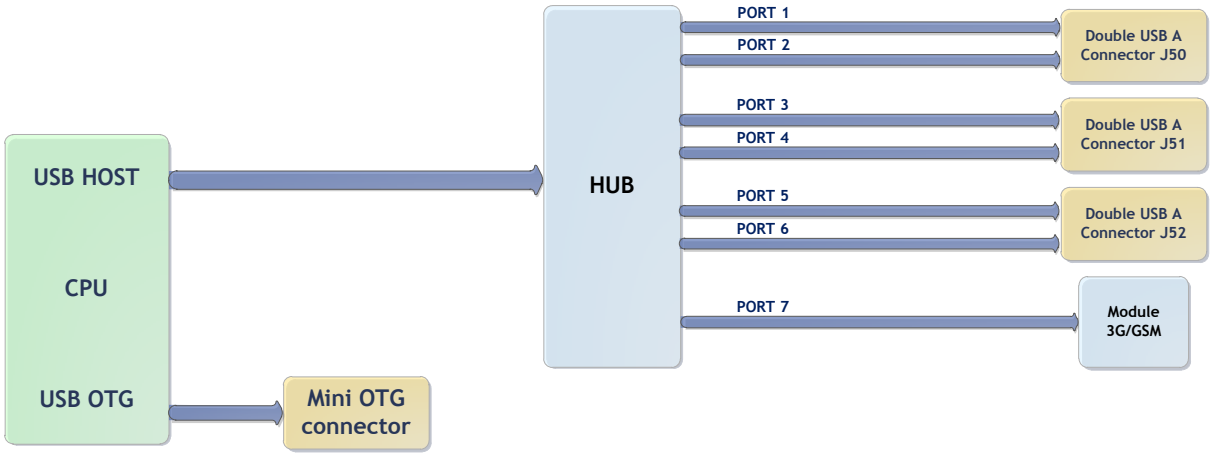


Figure 8 - USB Sub-system

[6] Board-To-Board connector used to link the CPU and the FPGA boards together.

3.5 CLOCKING CIRCUITRY

The REPTAR board's clocking circuitry is designed to be simple, reliable and easy to use.

Two separate 100MHz oscillators are used to drive the clocking trees of the Spartan6 and the Spartan3AN.

A slow oscillator at 25MHz is available for both FPGAs.

Separate oscillators provide stable references for the Spartan6 device's phase-locked loops (PLLs). These dedicated PLLs are used to distribute the PCI Express (125MHz), SATA (150MHz) clocks and DDR2 MCB blocs (not illustrated below).

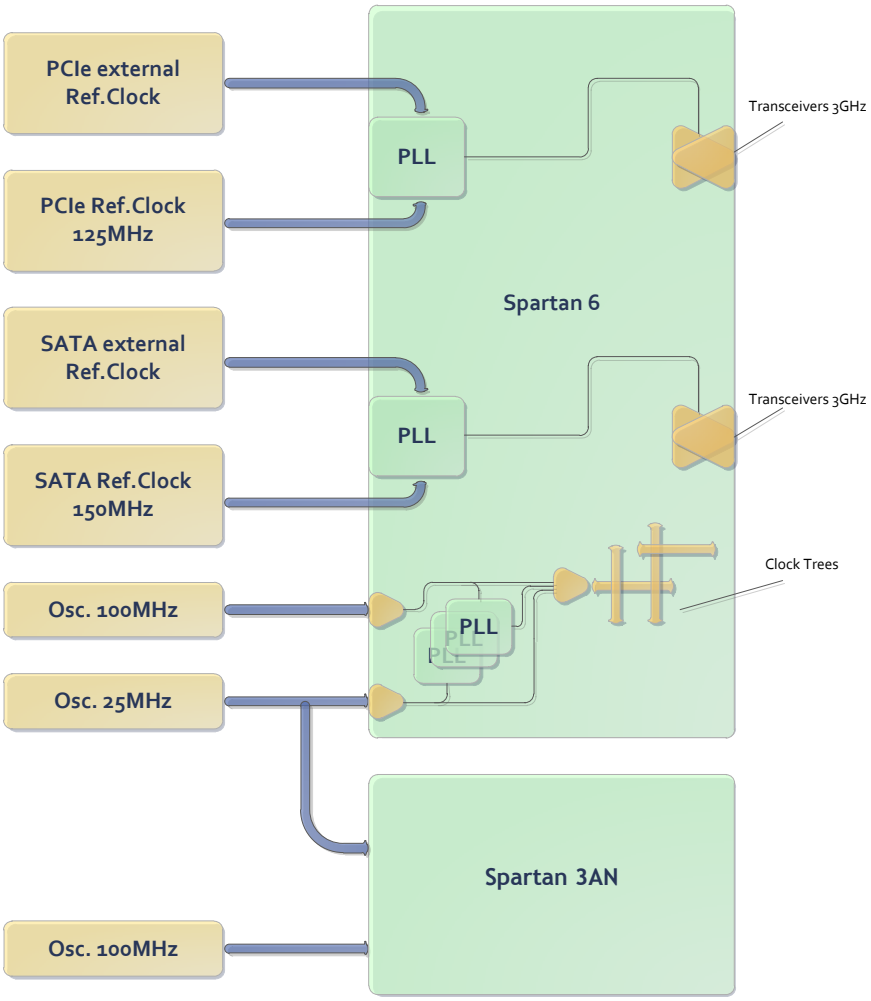


Figure 9 – Spartan6 Clocks sub-system

3.6 JTAG CHAINS

3.6.1 FPGA

The configuration JTAG chain illustrated below is constituted of the following components:

- FMC2 connector
- FMC1 connector
- Xilinx PlatformFlash
- Xilinx Spartan6

This chain can be driven, through a discrete mux (controlled by the Spartan3AN), either by a standard 14-Pin connector or by a USB-JTAG module from Digilent (www.digilent.com).

The Digilent module allows connecting the REPTAR board directly to the Xilinx Impact programming tool using a simple USB cable.

It is also possible to use a standard Xilinx USB Platform Cable connected to the 14-Pin connector.

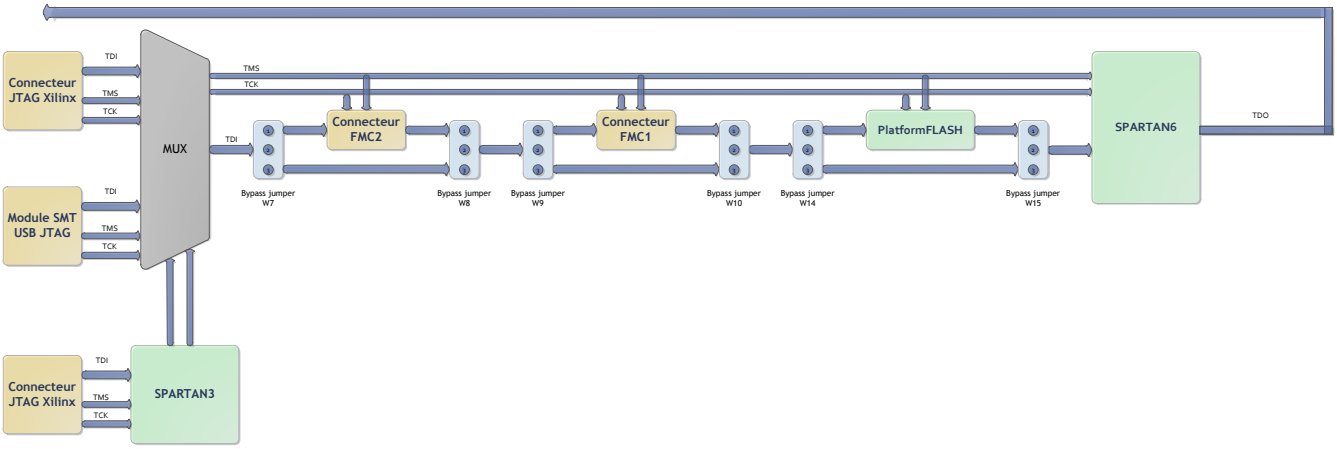


Figure 10 - JTAG Chain

A second JTAG chain exists to program the Spartan3AN, only.

3.6.2 CPU

The JTAG chain for the CPU is mainly used to perform debugging with specific tools, such as Code Composer Studio. The JTAG connector onto the CPU board is compliant with TI emulators.

4. DIMENSIONS

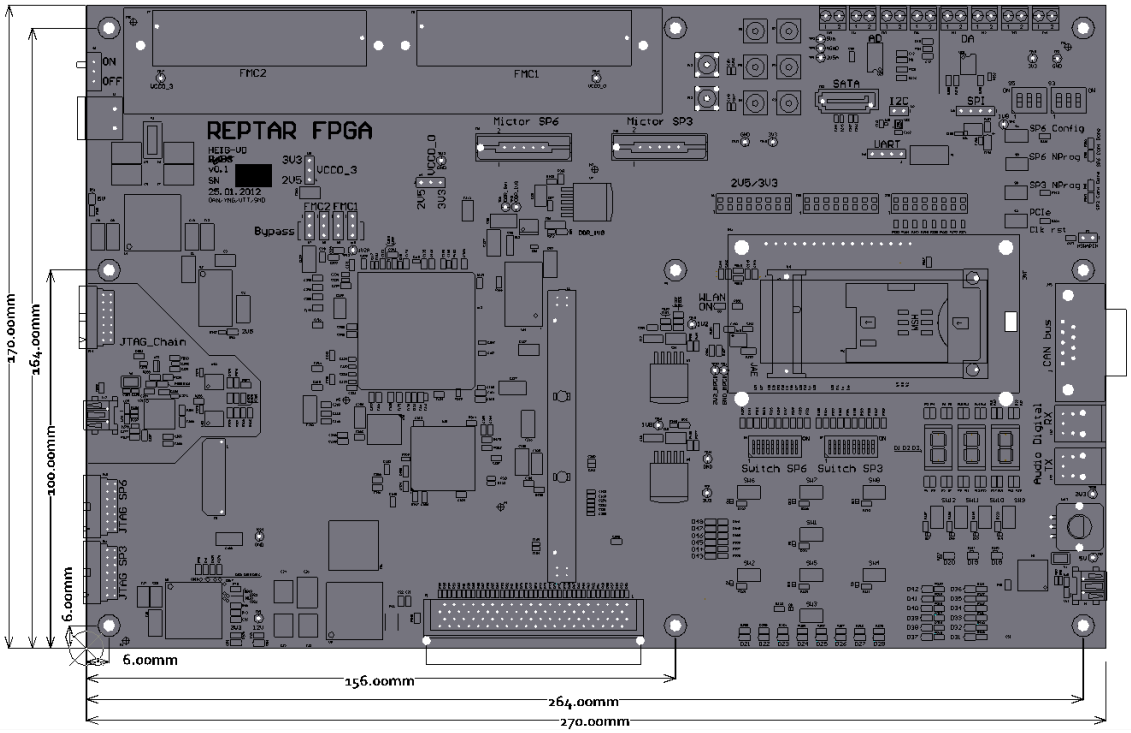


Figure 11 - FPGA Board dimensions

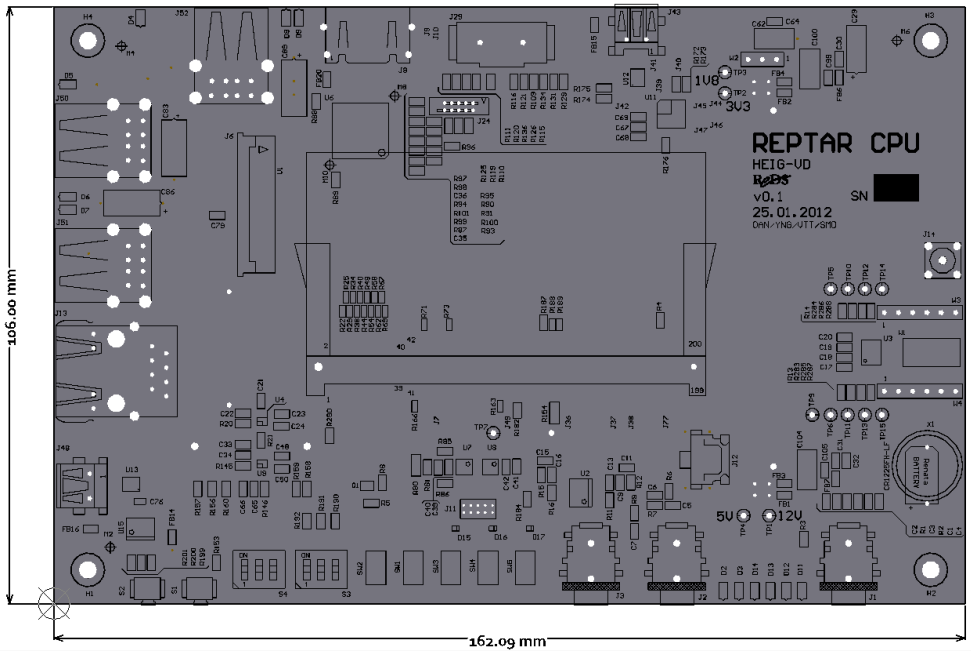


Figure 12 - CPU Board dimensions

This side view shows from bottom to top:

- Plexiglas Support
- FPGA mainboard
- CPU board
- 7" display (at 30°)

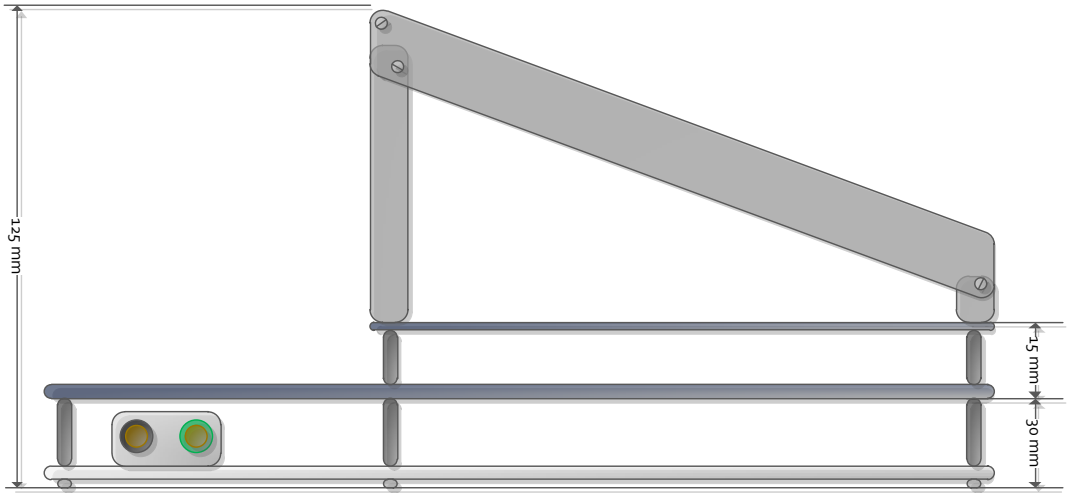


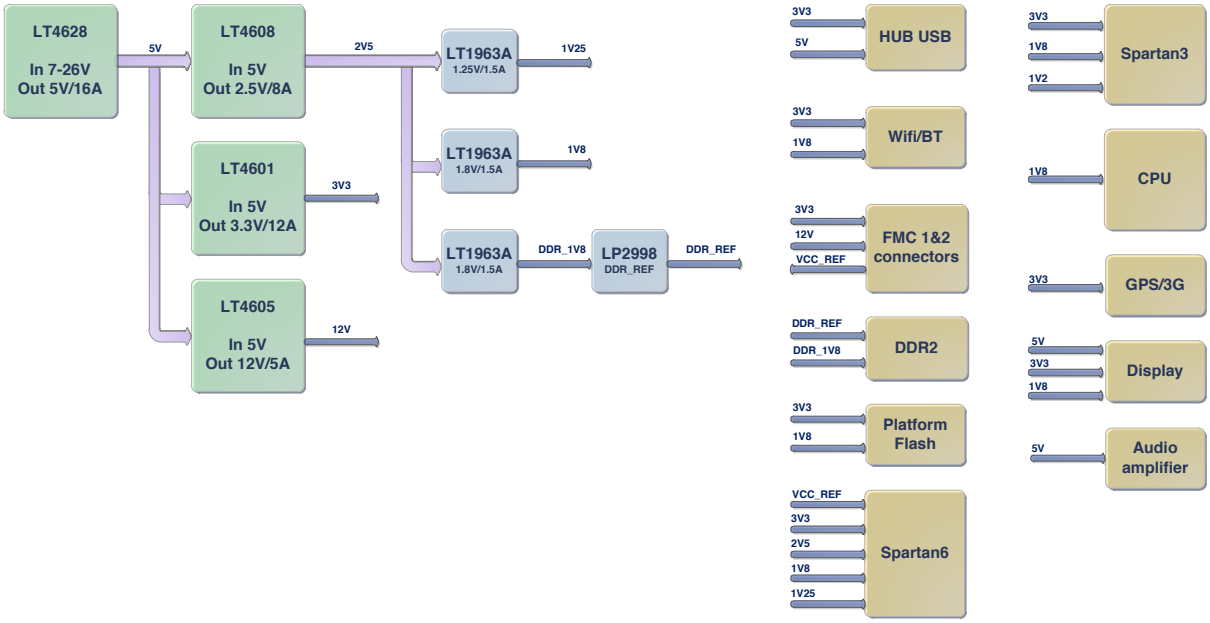
Figure 13 - REPTAR Board side view

5. POWER SUPPLIES

The main circuitry is a Linear Technologies µModule LT4628. It supports an input voltage between 7V and 26V and generates a main 5V/16A output for the other regulators.

Altogether, including two FMC boards connected to the board, REPTAR will consume around 80 Watt.

The image below shows the power supplies of the REPTAR board and the main peripherals powered by them.



6. ADDITIONAL INFORMATION

6.1 REVISION HISTORY

Chapter	Date	Version	Changes Made
All	June 2012	1.0	▪ First publication /Proto1 (v0.1)
All	Sept 2012	1.1	▪ Modifications for Proto2 (v1.0)

Table 2 - Revision History

6.2 CONTACT

For the most up-to-date information about the REPTAR board, refer to the REDS wiki at wikireds.heig-vd.ch

Or, contact the REDS institute directly:

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