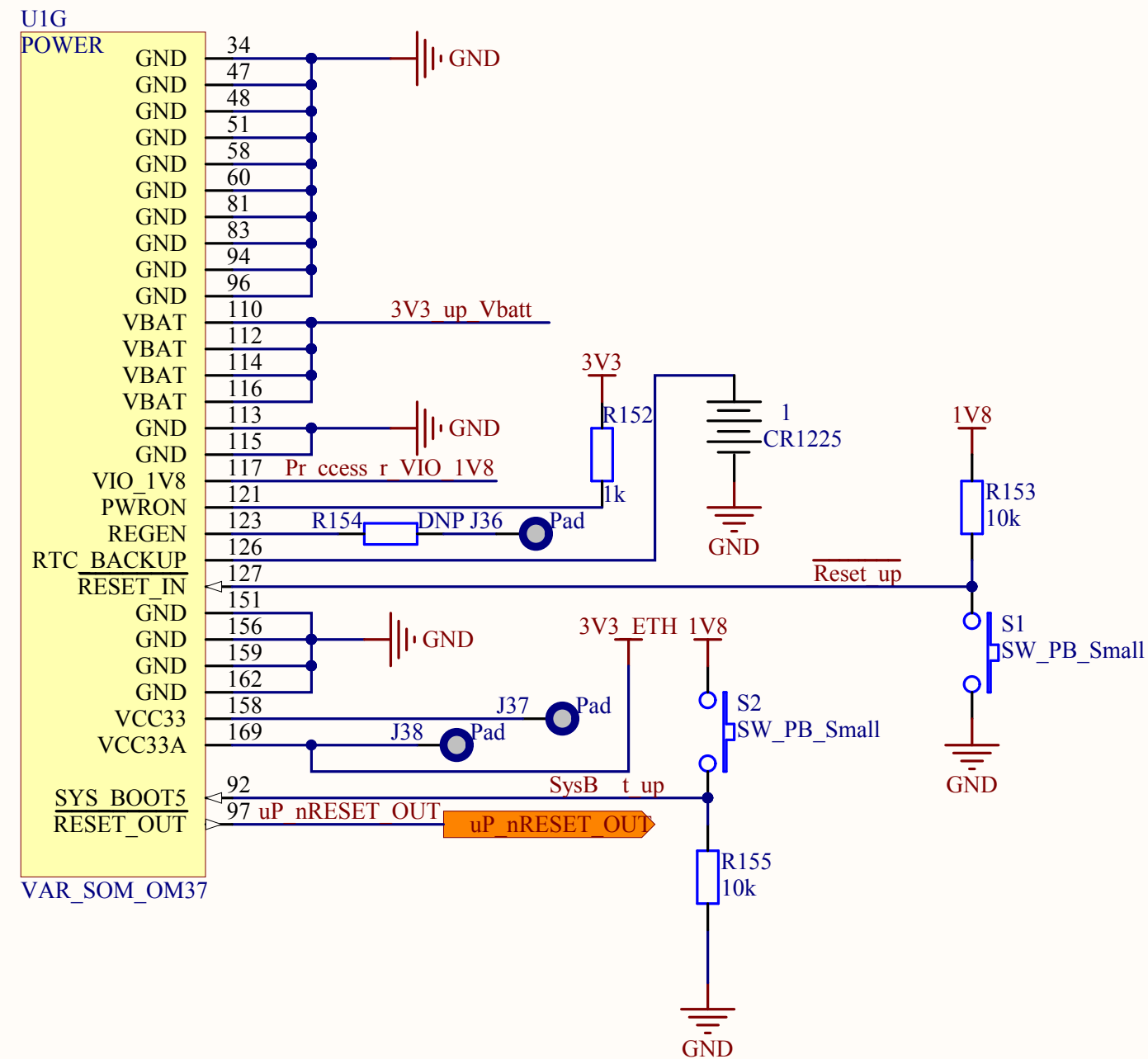
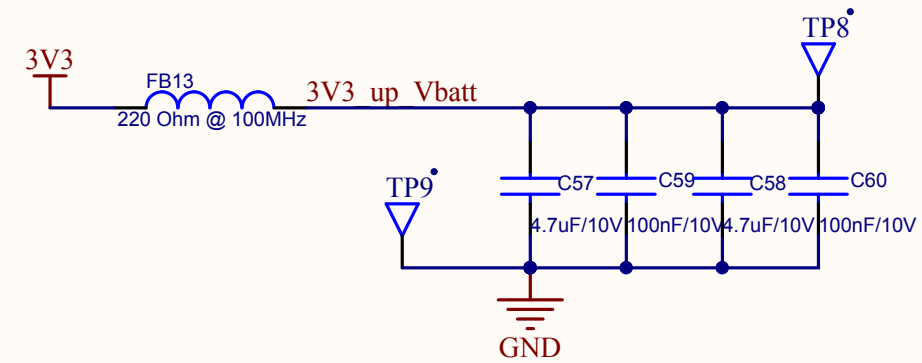


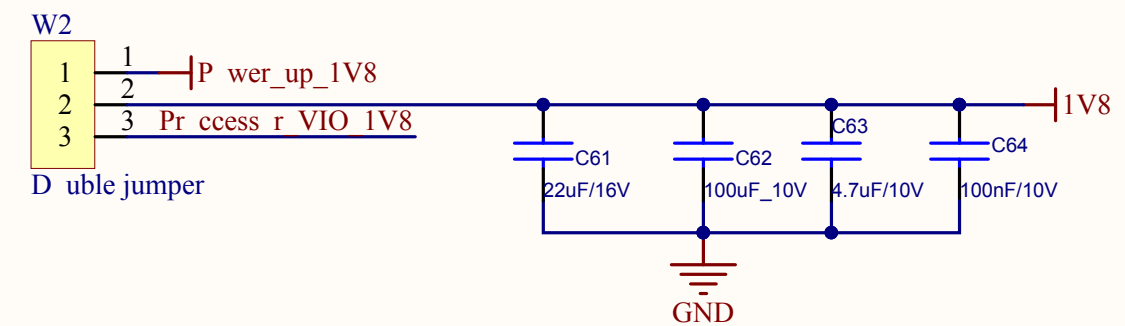
Revisi n OK 03.10.2012 OAN/VTT



3V3 pr ccess r v ltage

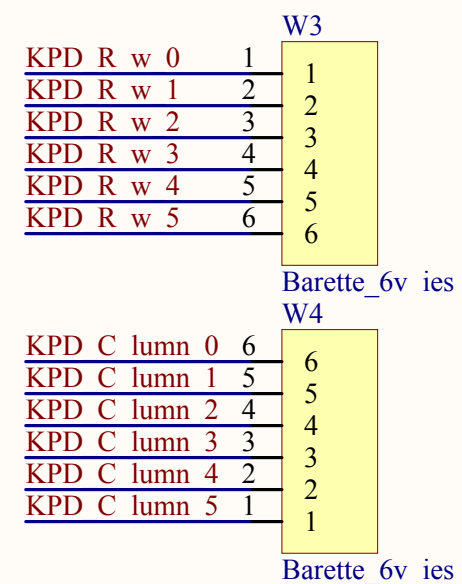
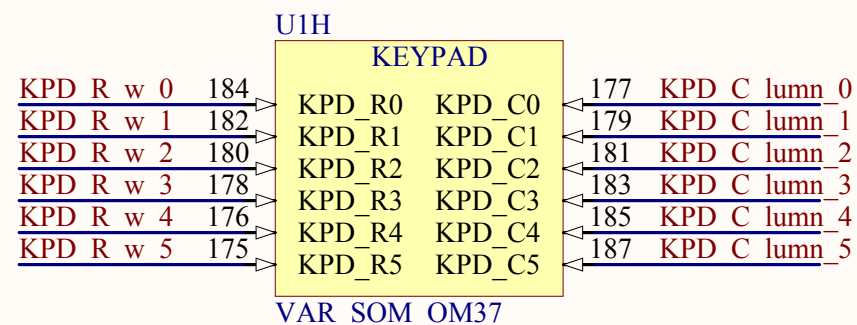


1V8 pr cces r b ard s urce v ltage selecti n



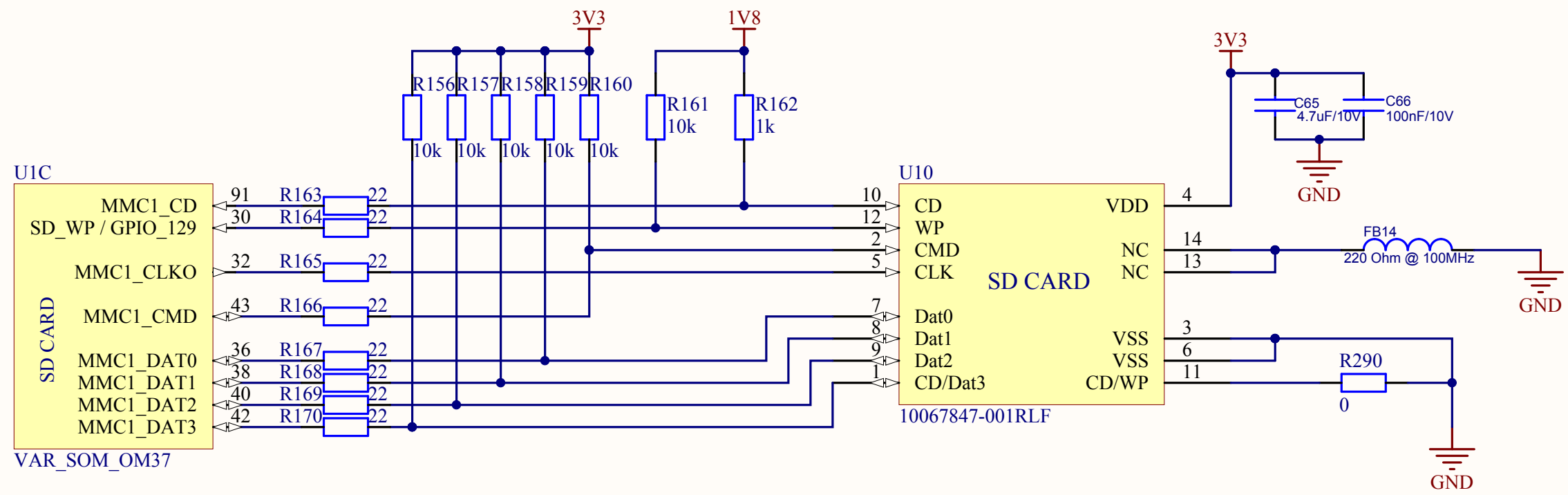
Questi n (03.10.2012)
Est-il ncessaire de garder cette f ncti nnalit ?

Reserved functi n

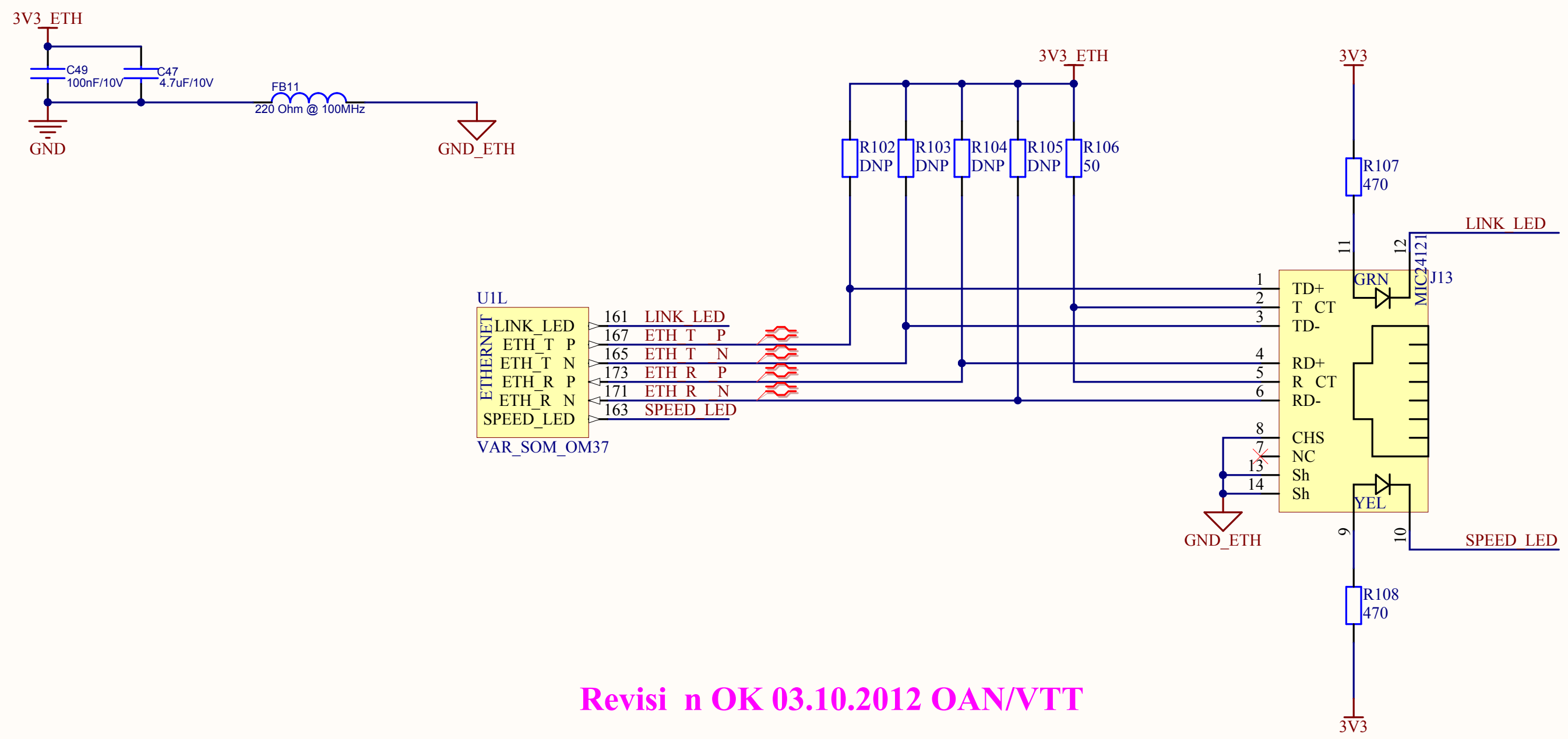


Reds PCB_DM3730.PrjPCB	
DM3730_POWER.SchD c	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Appr ved by: *	Page 18 f 28

Revisi n OK 03.10.2012 OAN/VTT



Reds PCB_DM3730.PrjPCB	
DM3730_SDCARD.SchD c	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Appr ved by: *	Page 19 f 28



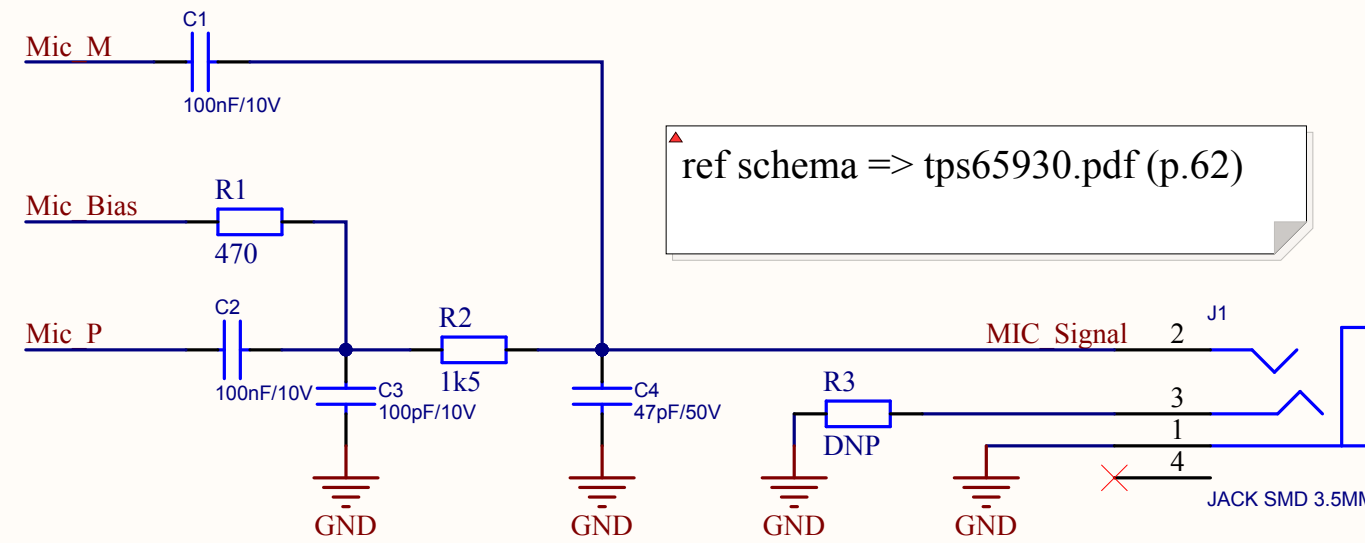
Revisi n OK 03.10.2012 OAN/VTT

RODS PCB_DM3730.PrjPCB	
DM3730_ETHERNET.SchD c	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Appr ved by: *	Page 20 f 28

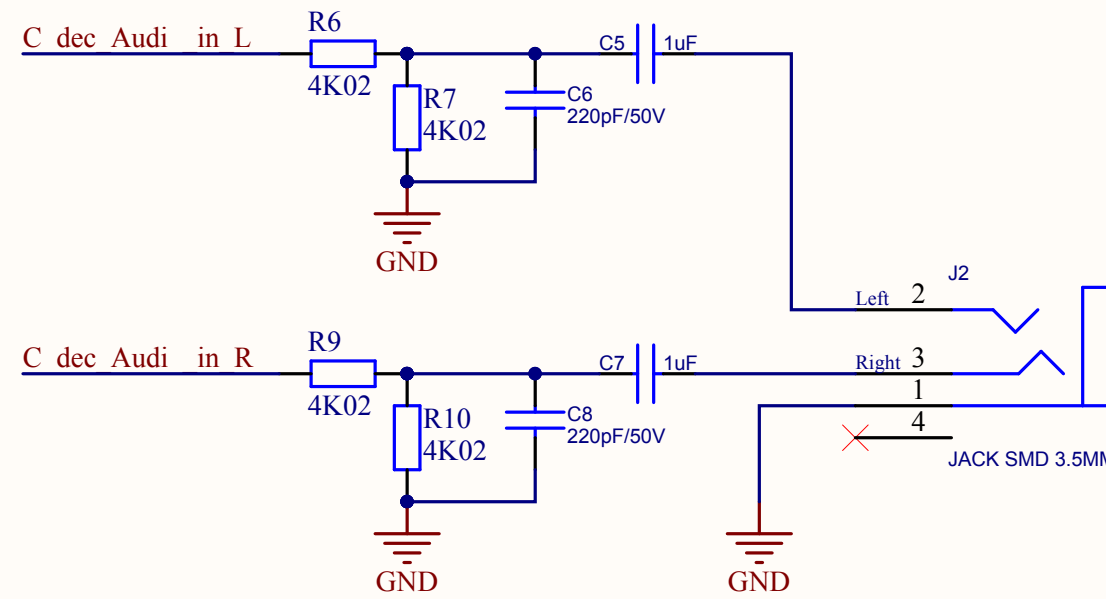
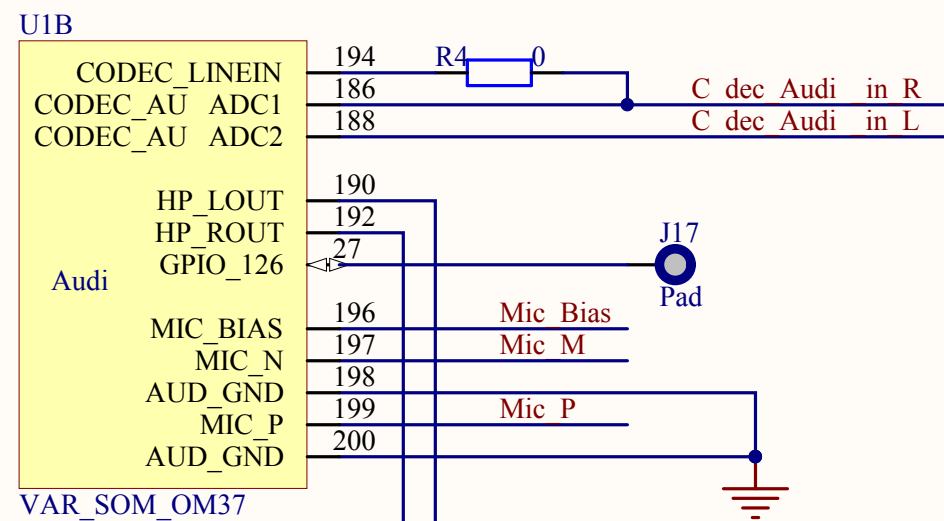
Revisi n OK 03.10.2012 OAN/VTT

Note:

Le blindage du chemin MIC et AUDIO IN a été amélioré au niveau du PCB - A valider

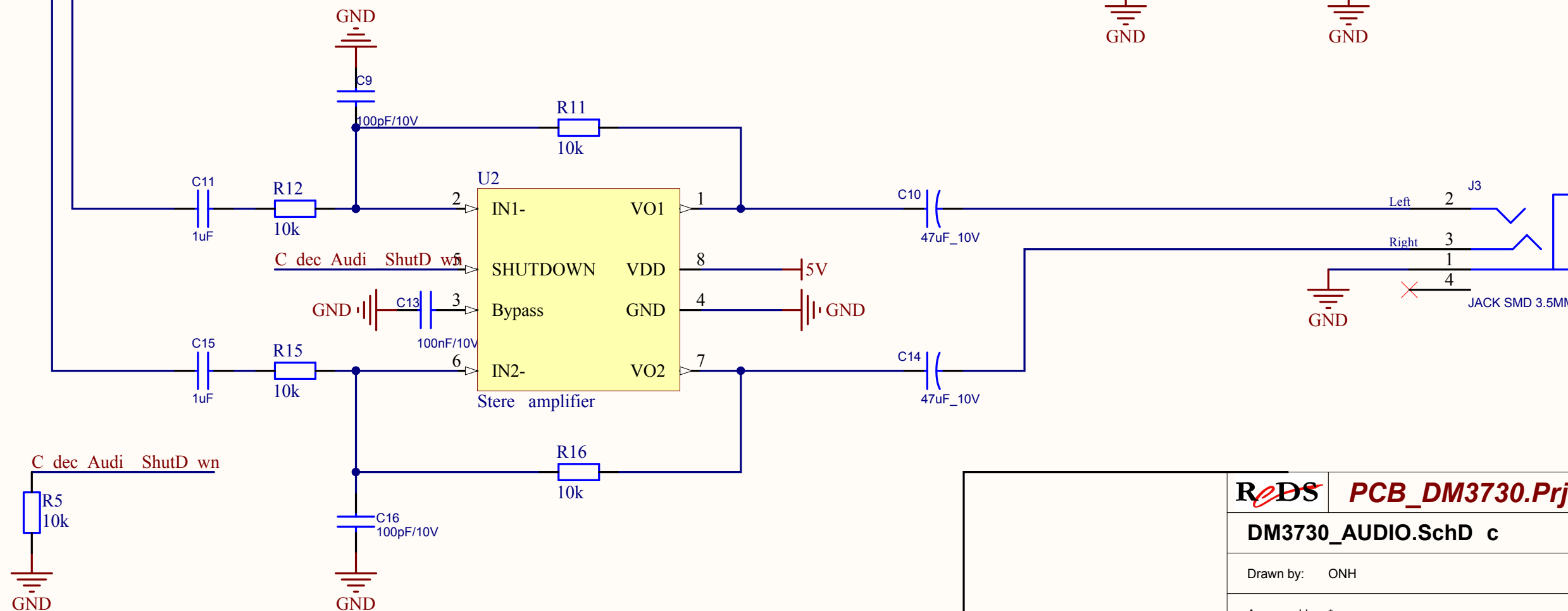
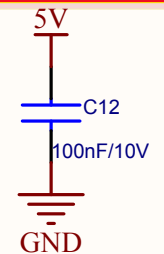


MICROPHONE



AUDIO IN

Dec uplage A placer vers U2



AUDIO OUT

PCB_DM3730.PrjPCB

DM3730_AUDIO.SchD c

Drawn by: ONH

Appr ved by: *

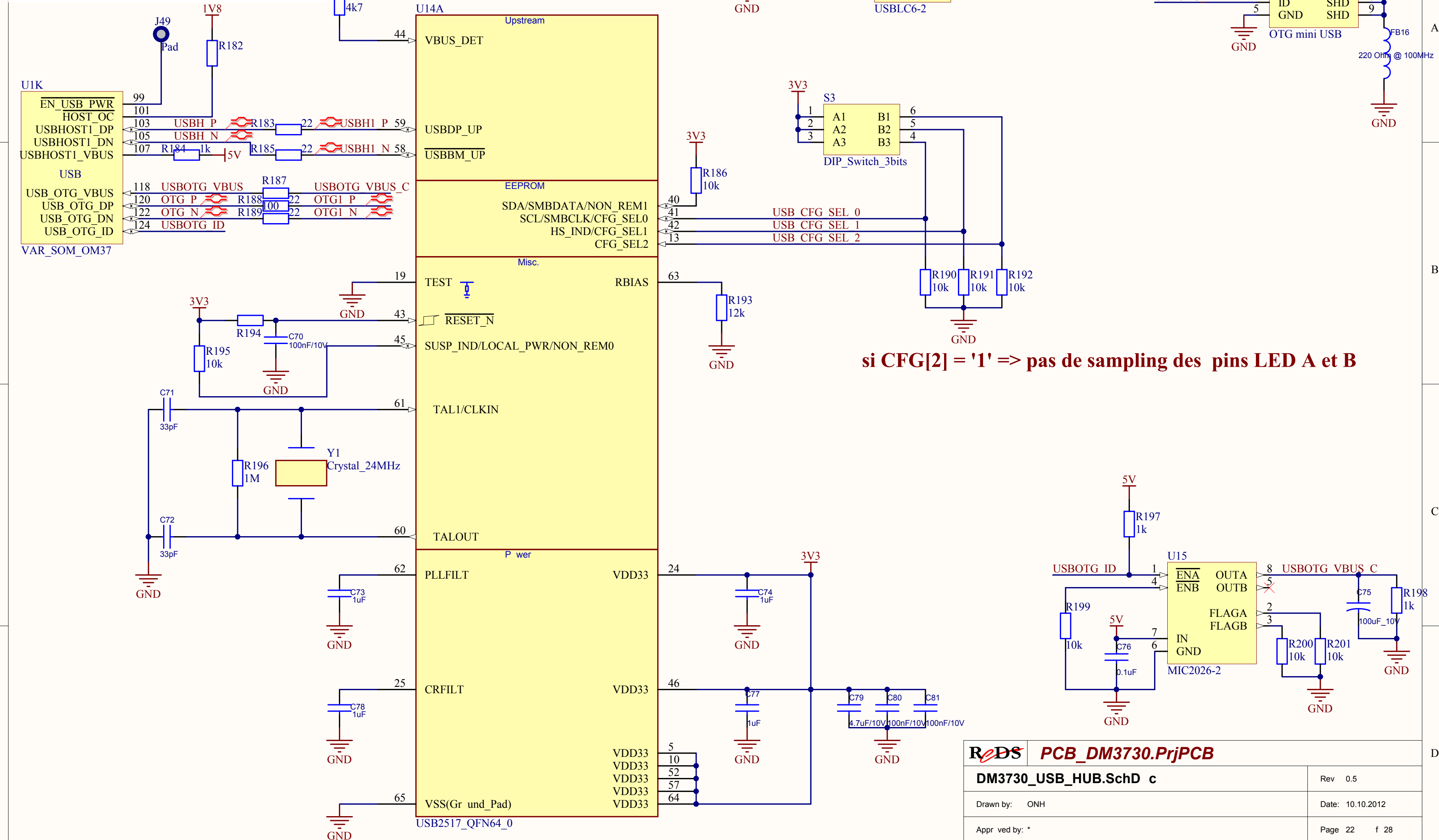
Rev 0.5

Date: 10.10.2012

Page 21 f 28

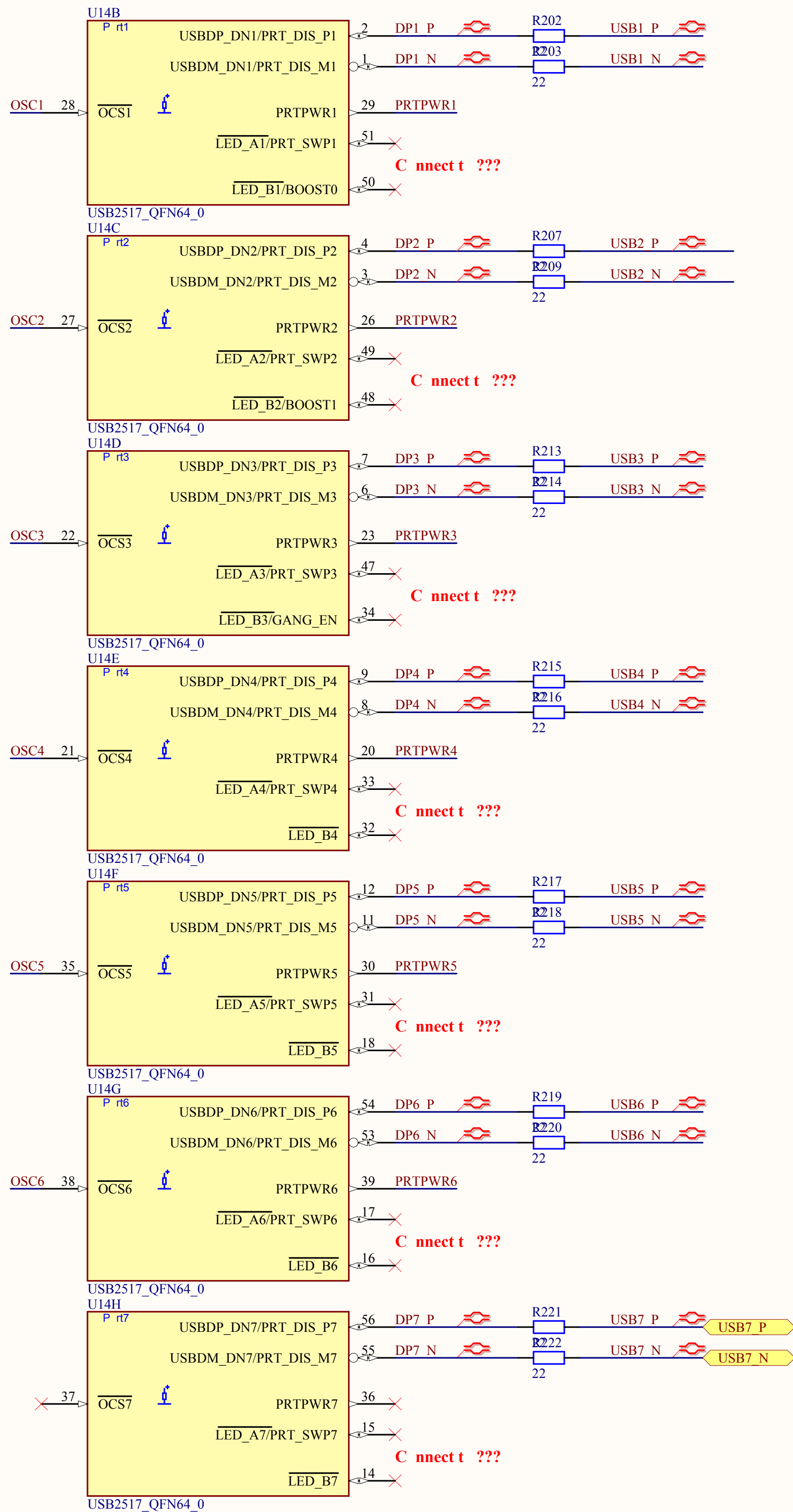
**NOTE: OTG fonctionnelle en mode Device -
 Testé et validé. En mode Master, pas validé et
 fonctionnalité supprimée des specs.
 => A supprimer dans Datasheet**

Revisi n OK 03.10.2012 OAN/VTT

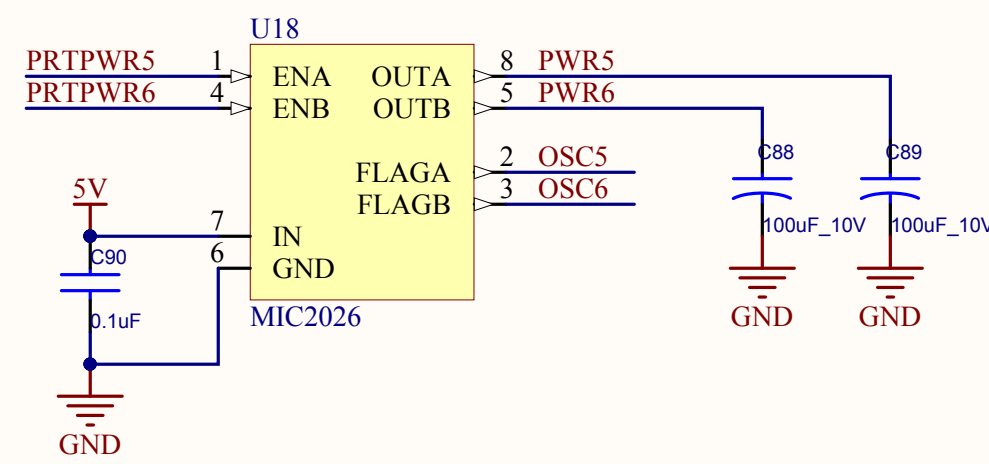
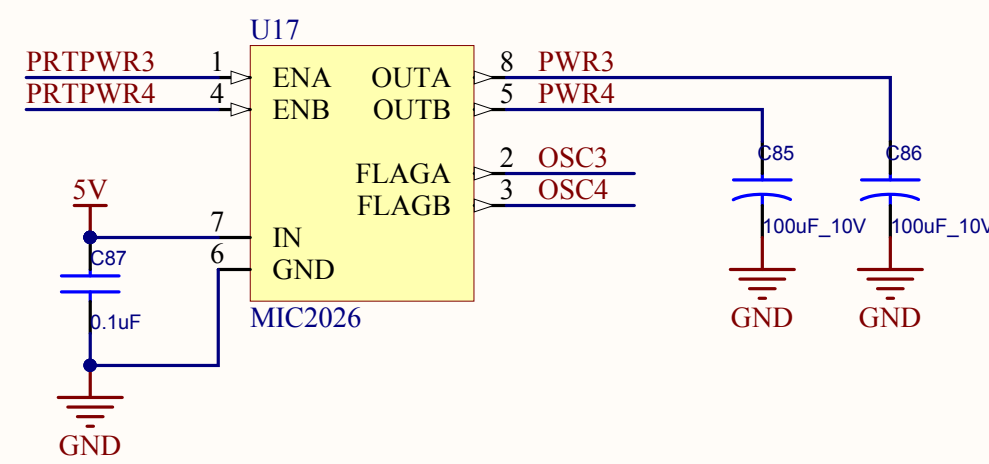
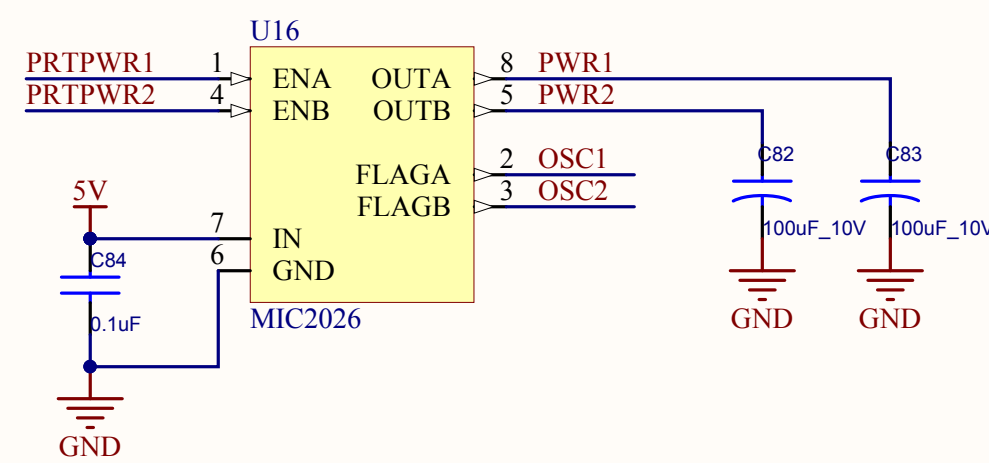


si CFG[2] = '1' => pas de sampling des pins LED A et B

RODS PCB_DM3730.PrjPCB	
DM3730_USB_HUB.SchD c	
Drawn by: ONH	Rev 0.5
Appr ved by: *	Date: 10.10.2012
	Page 22 f 28

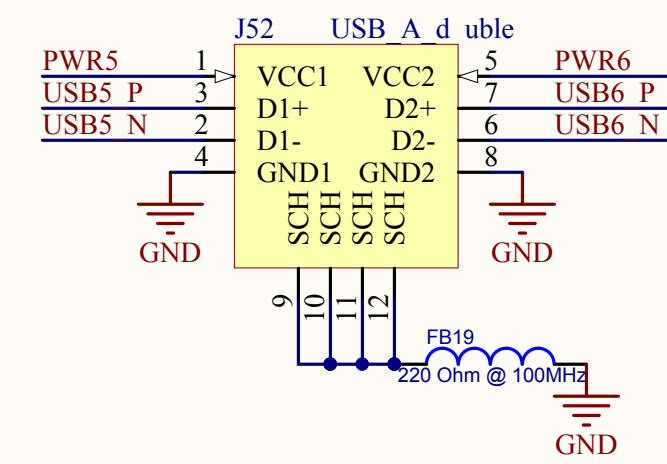
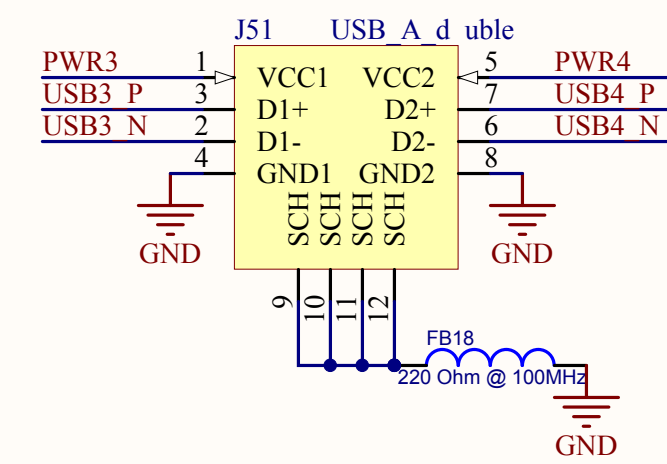
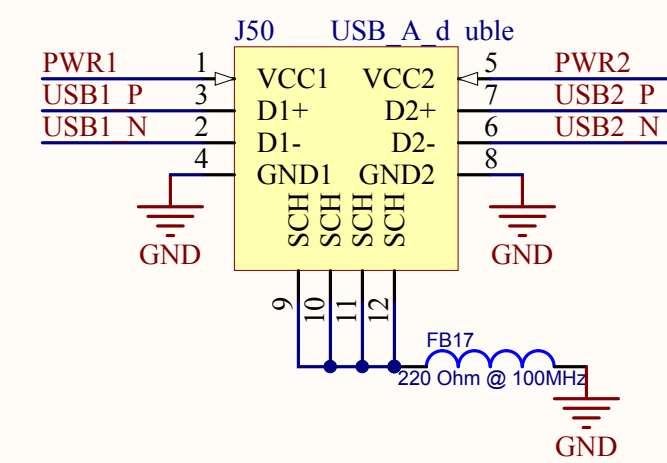


USB p r tecti n

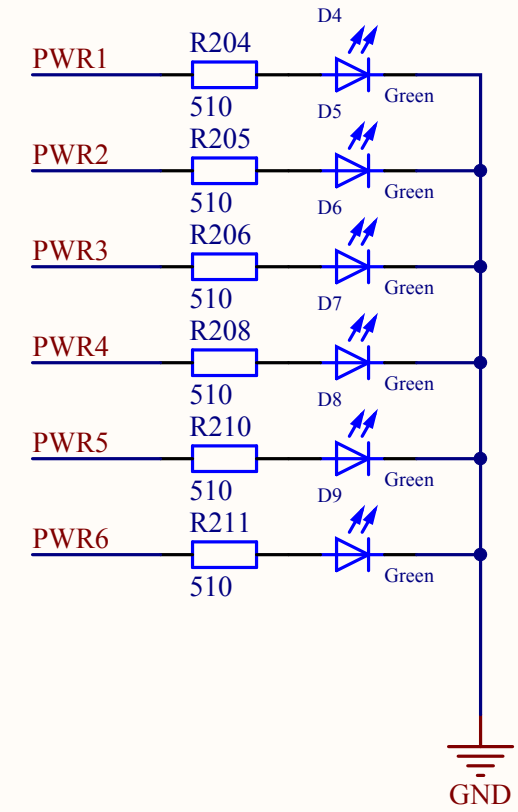


3G/GPS CONNECTION

USB c nnect rs



USB p w r inf

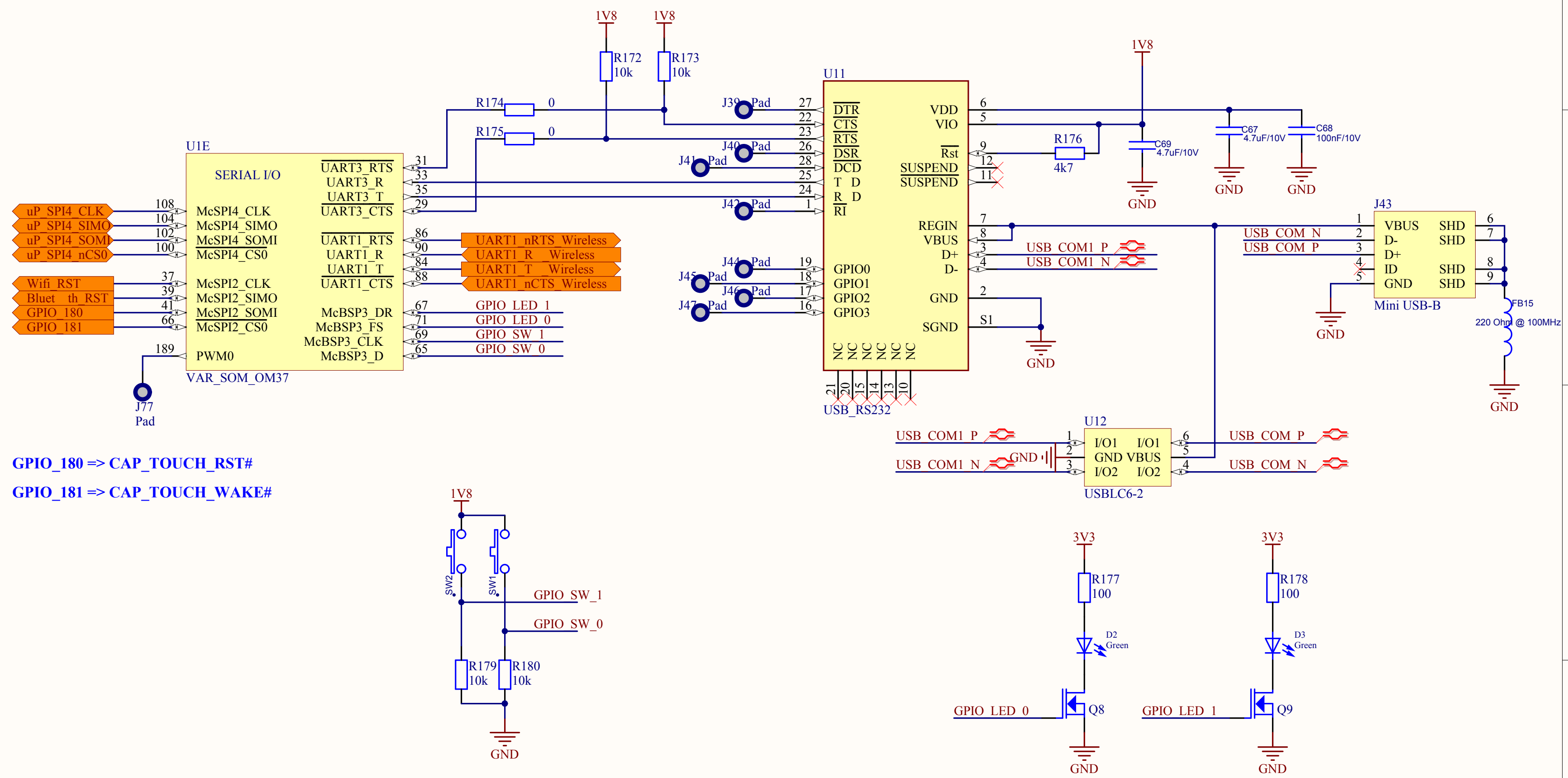


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ReDS	PCB_DM3730.PrjPCB
DM3730_USB_PERIPHERAL.Schd c	
Drawn by: ONH	Rev 0.5
Appr ved by: *	Date: 10.10.2012
	Page 23 f 28

C rresp ndance SPI FPGA <=> CPU
 SP6_SPI_SDO <=> up_SPI_SIMO (Slave In Master Out)
 SP6_SPI_SDIO <=> up_SPI_SOMI (Slave Out Master In)

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GPIO_180 => CAP_TOUCH_RST#
 GPIO_181 => CAP_TOUCH_WAKE#

PCB_DM3730.PrjPCB	
DM3730_SERIAL.SchD c	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Appr ved by: *	Page 24 f 28

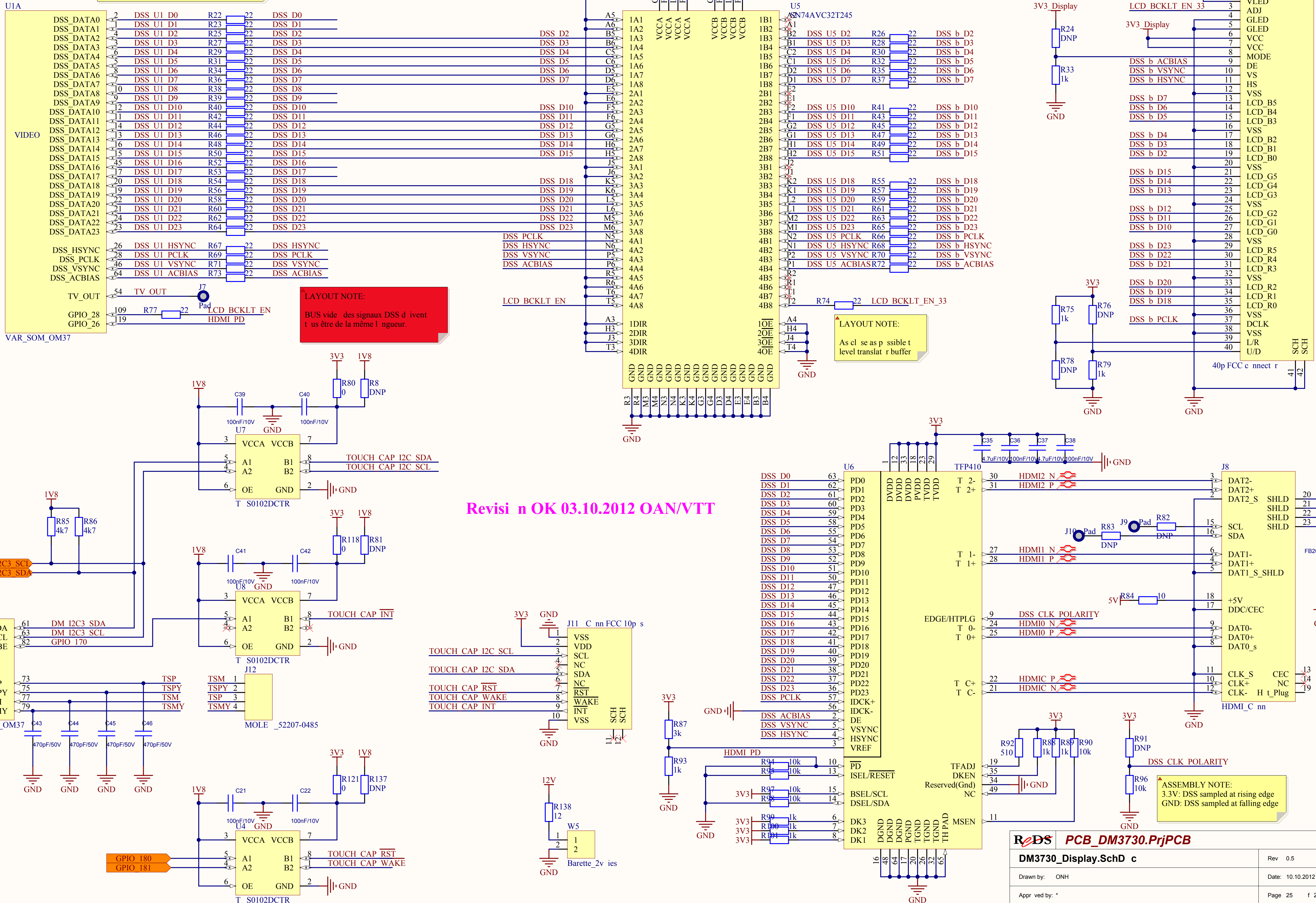
LAYOUT NOTE:
As cl se as p ssible t SODIMM c nnect r

LAYOUT NOTE:
BUS vide des signaux DSS d ivent t us être de la même l ngeur.

LAYOUT NOTE:
As cl se as p ssible t level translat r buffer

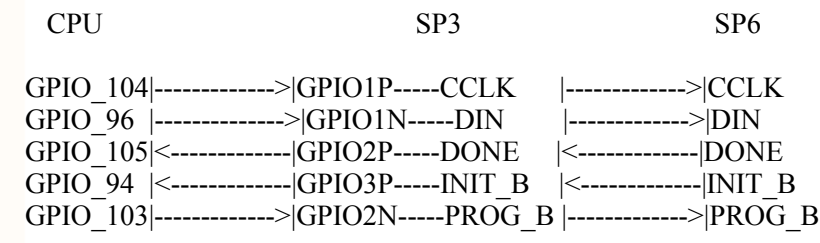
ASSEMBLY NOTE:
3.3V: DSS sampled at rising edge
GND: DSS sampled at falling edge

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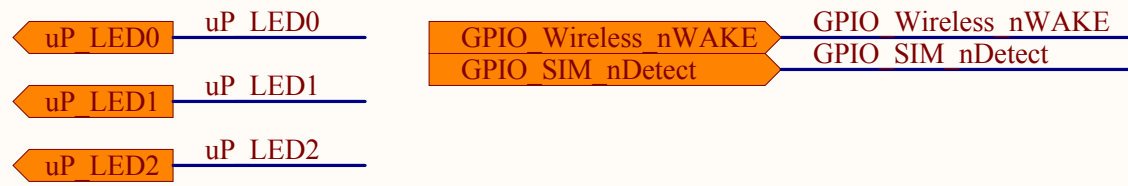
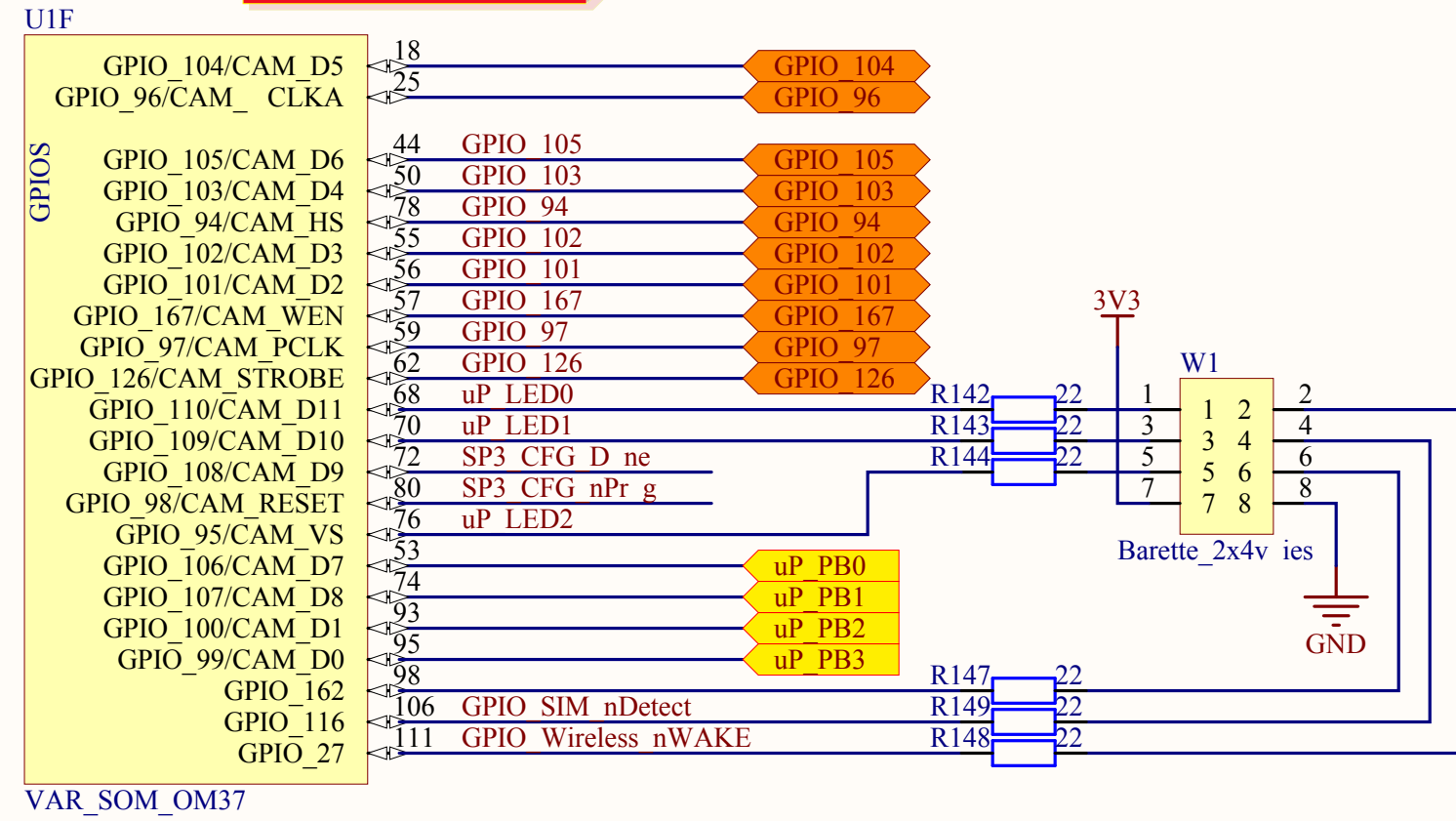
ReDS PCB_DM3730.PrjPCB	
DM3730_Display.SchD c	
Drawn by: ONH	Rev 0.5
Appr ved by: *	Date: 10.10.2012
	Page 25 of 28

Connexion SP6 (slave Serial connections)

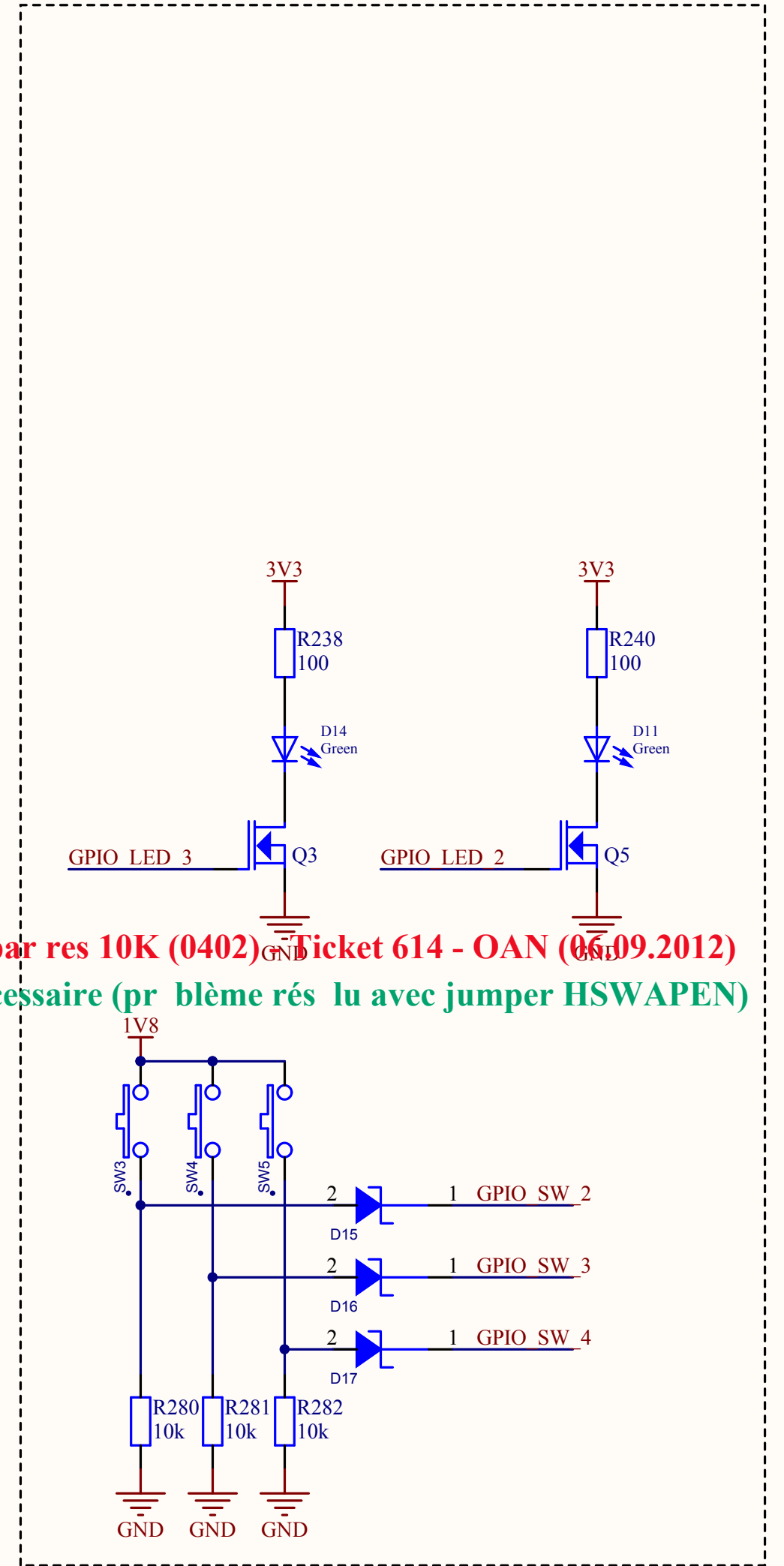
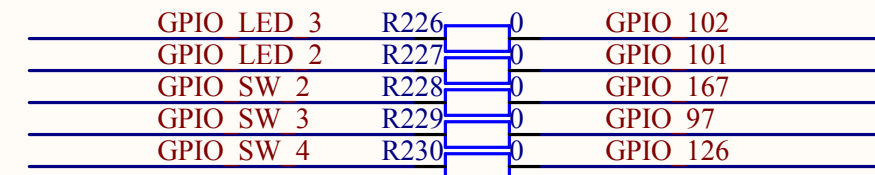


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Tous les signaux de UIF peuvent être swapper entre eux.

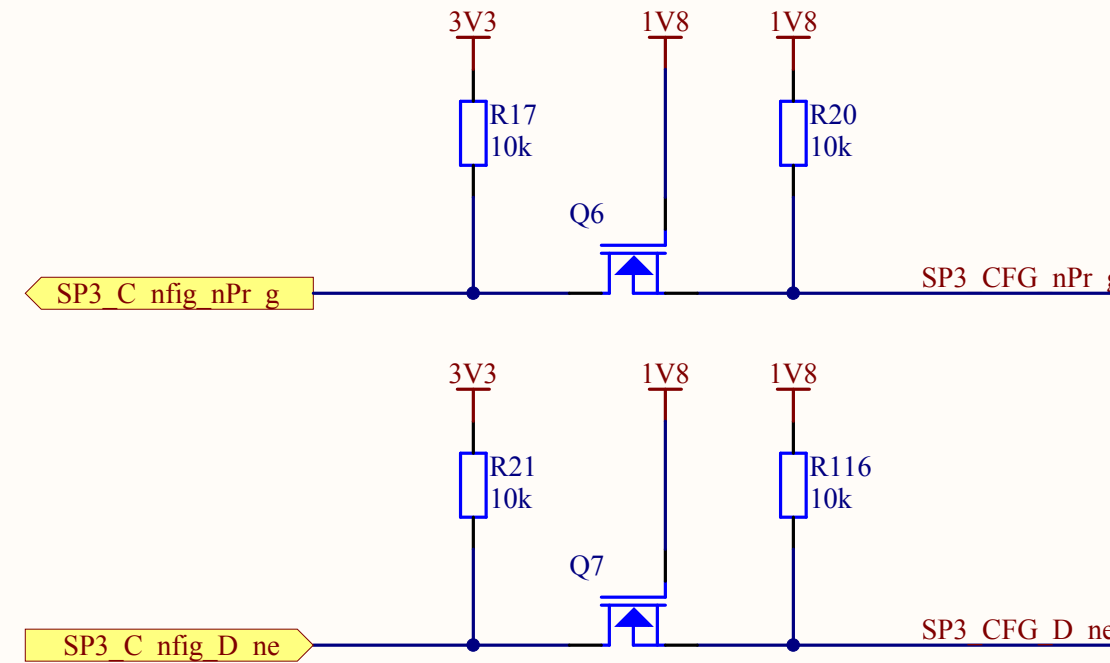
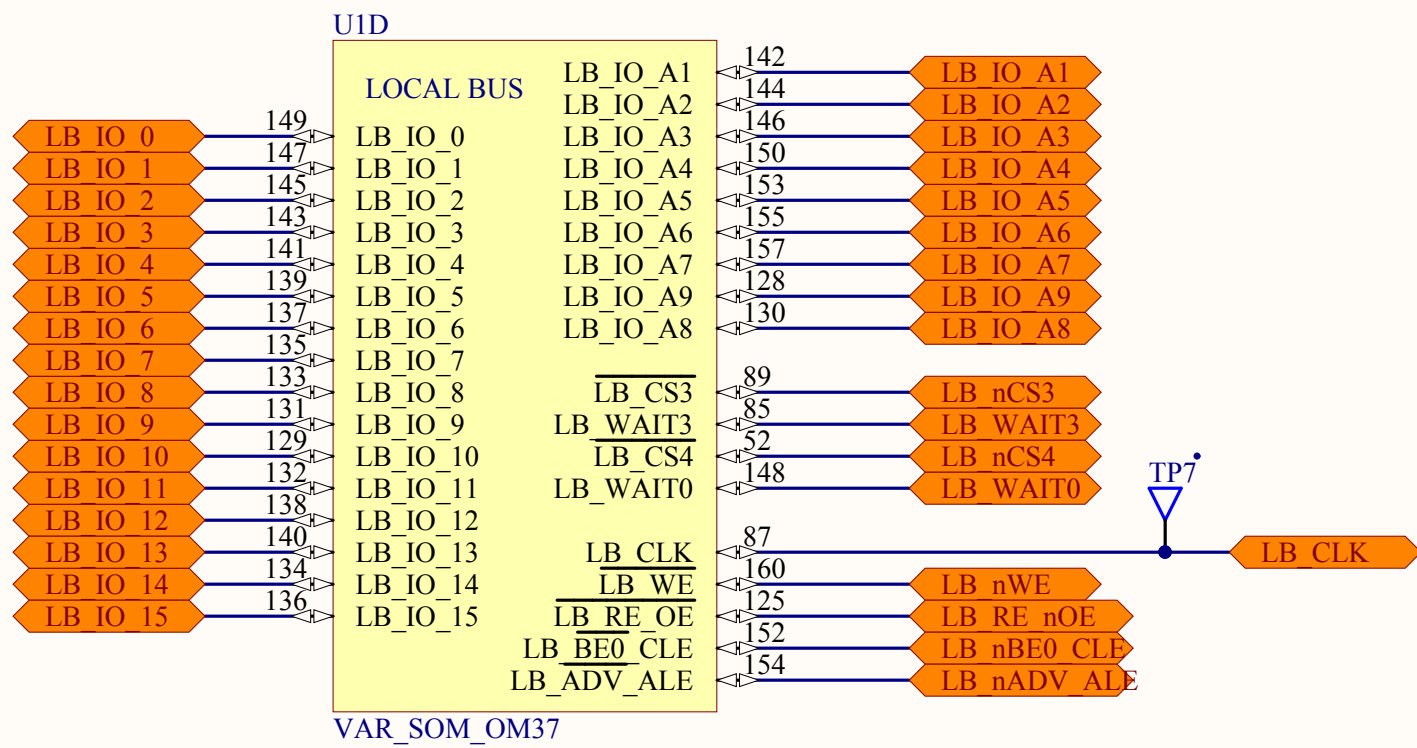


LED3 (GPIO_102) is c mm n with CPU, SP3 and SP6
LED2, SW2, SW3, SW4 is c mm n with CPU and SP6 nly

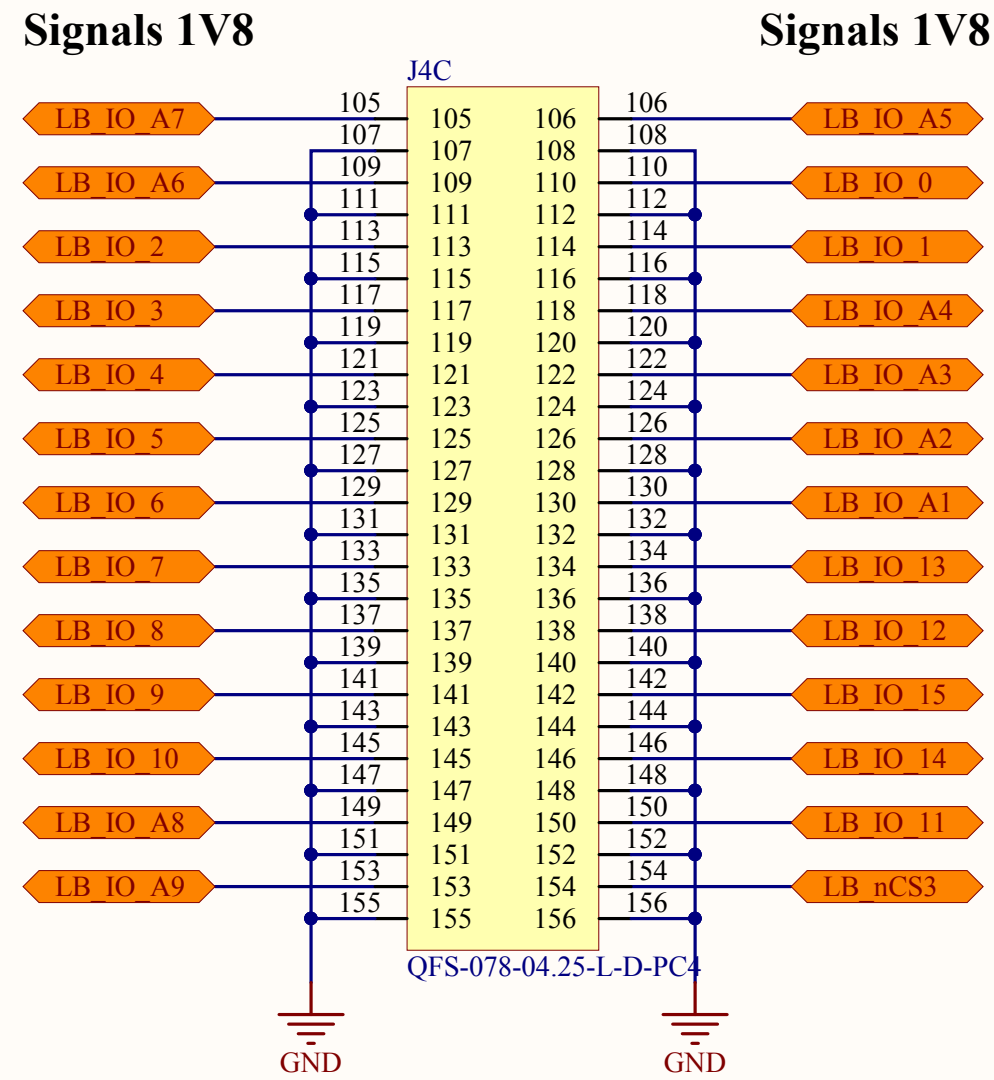


D15 à D17 à remplacer par res 10K (0402) Ticket 614 - OAN (06/09.2012)

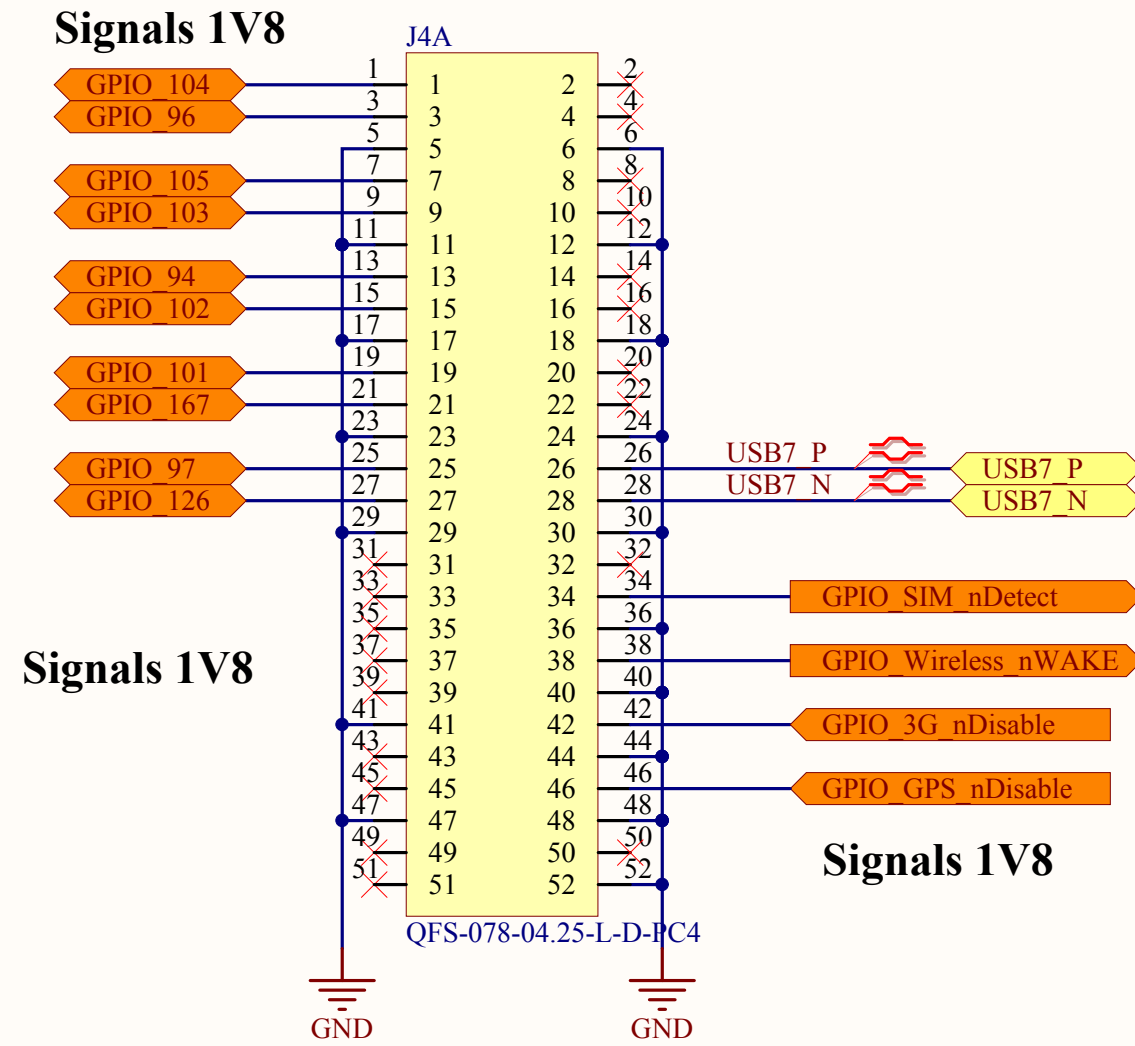
Ticket 614 - cl s - 03.10.2012 - pas de m dification nécessaire (pr blème rés lu avec jumper HSWAPEN)



uP local bus



GPIOs GPS 3G

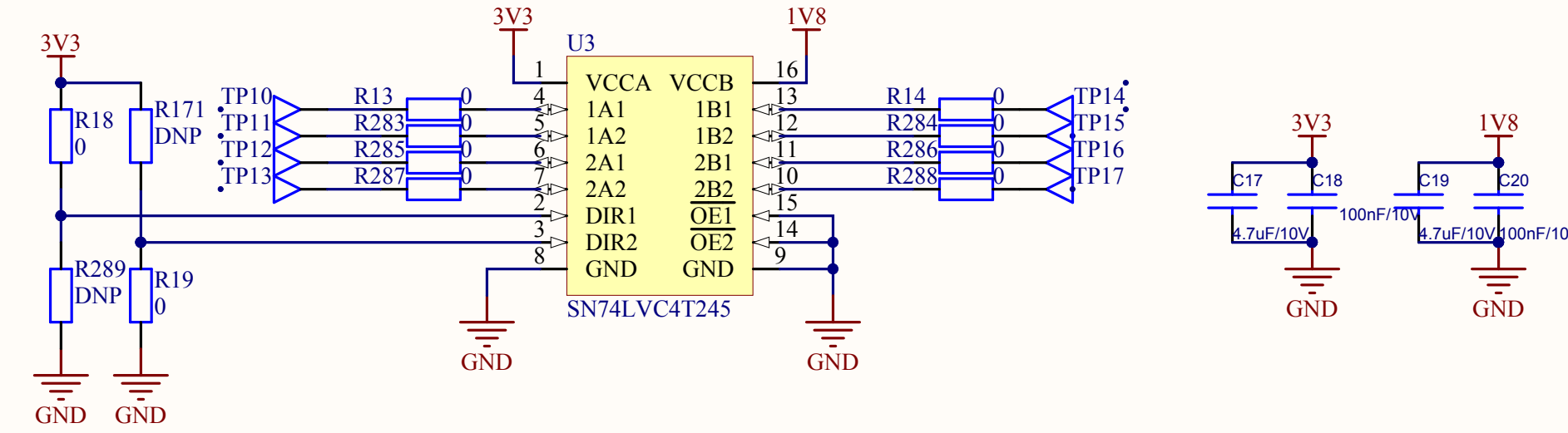


Lay out n te f r QSH_60 pins and QFS-078-04.25- -D-PC4 c nnect rs

LAYOUT NOTE:
- Each differential pair sh uld pr vide a differential impedance f 100 hm.
- Each single signal sh uld pr vide an impedance f 50 hm

uP GPIOs

Dir = 0 => B t A
Dir = 1 => A t B



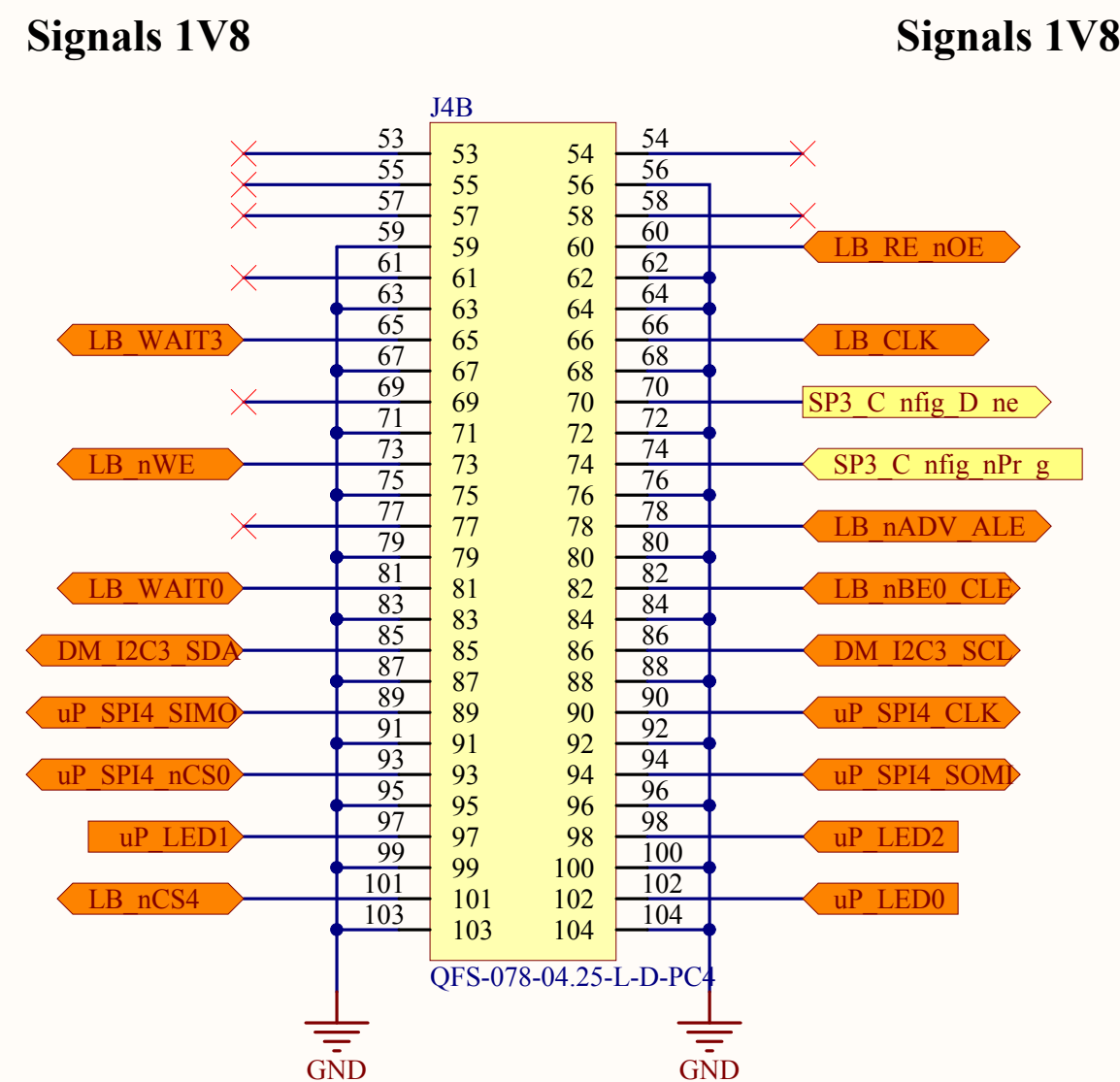
C nfig SP6 (slave Serial c nnecti ns)

CPU	SP3	SP6
GPIO_104	GPIO1P---CCLK	CCLK
GPIO_96	GPIO1N---DIN	DIN
GPIO_105	GPIO2P---DONE	DONE
GPIO_94	GPIO3P---INIT_B	INIT_B
GPIO_103	GPIO2N---PROG_B	PROG_B

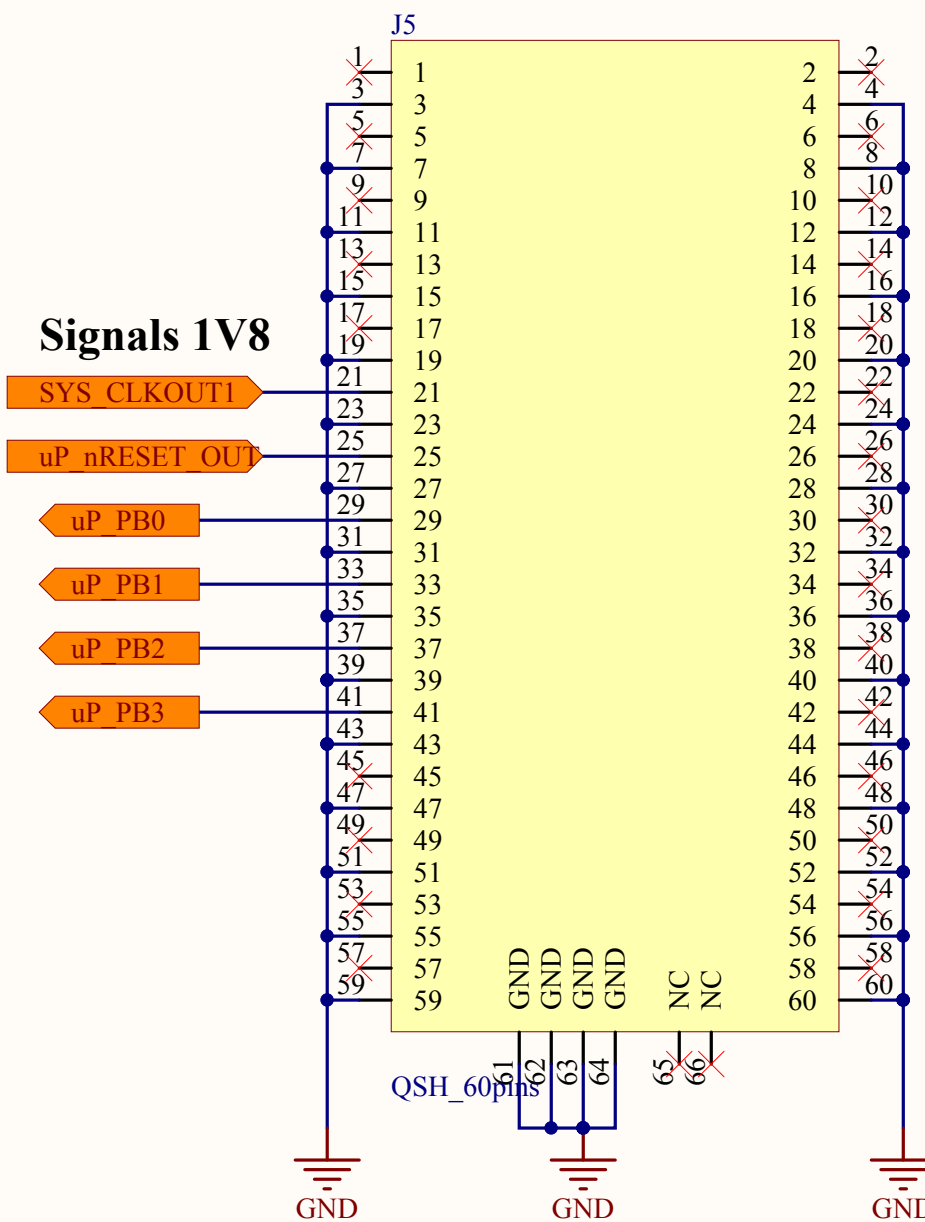
Ne rien changer au pin ut du c nnecteur car e rresp ndance avec carte uP!!!

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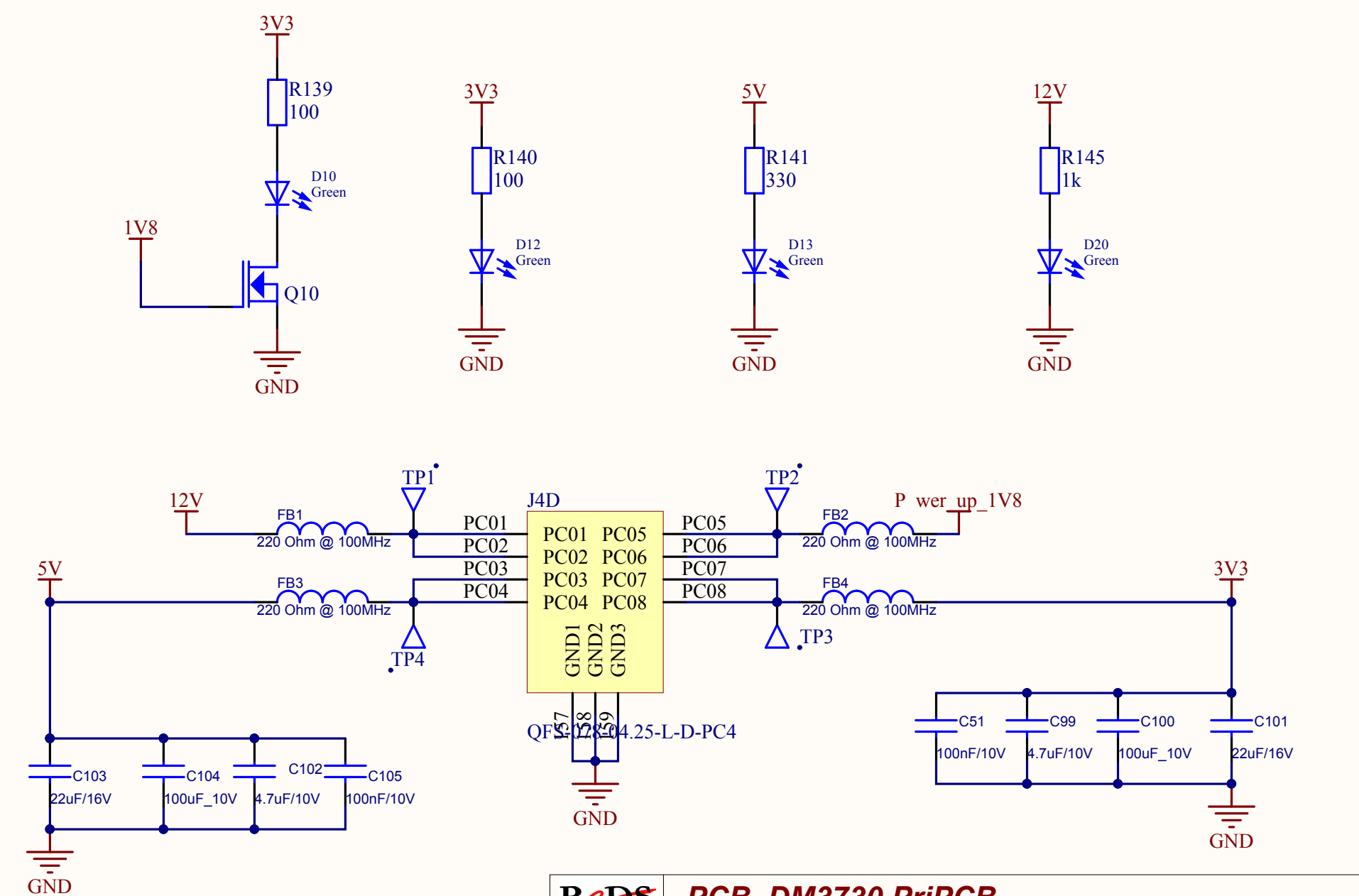
I2C UART uP_SWs uP_LEDs SPI



GPIOs SPI c nf



POWER



RedS	PCB_DM3730.PrjPCB
DM3730_BT_B_C nn.SchD c	
Drawn by: ONH	Rev 0.5
Appr ved by: *	Date: 10.10.2012
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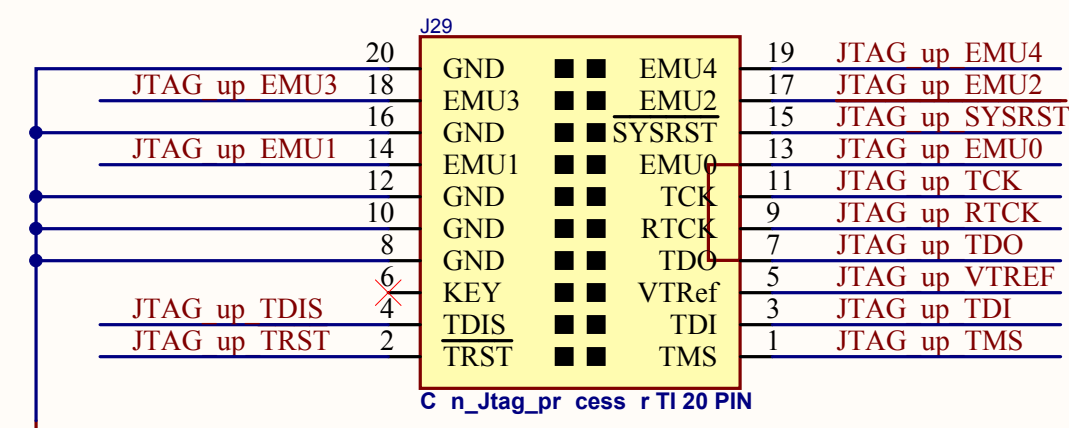
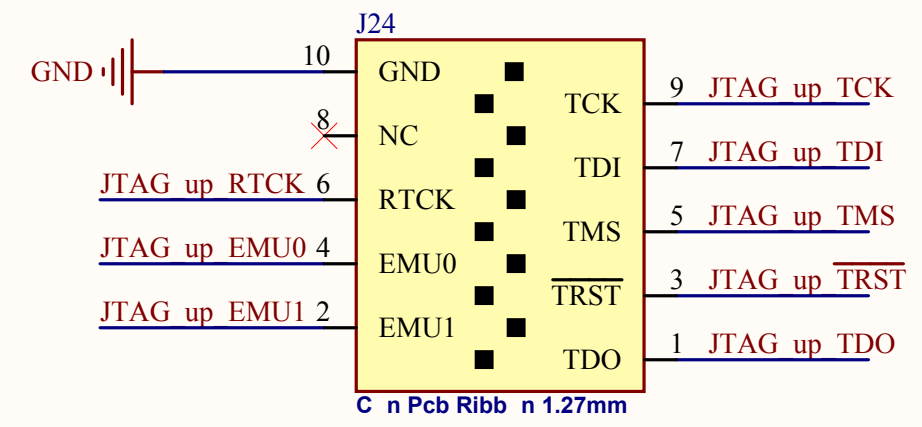
Barette pour carte processeur



Centre-connexion pour carte processeur

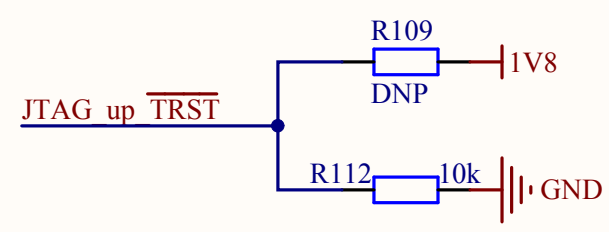


Centre-connexion Ribb n -> PCB FPGA

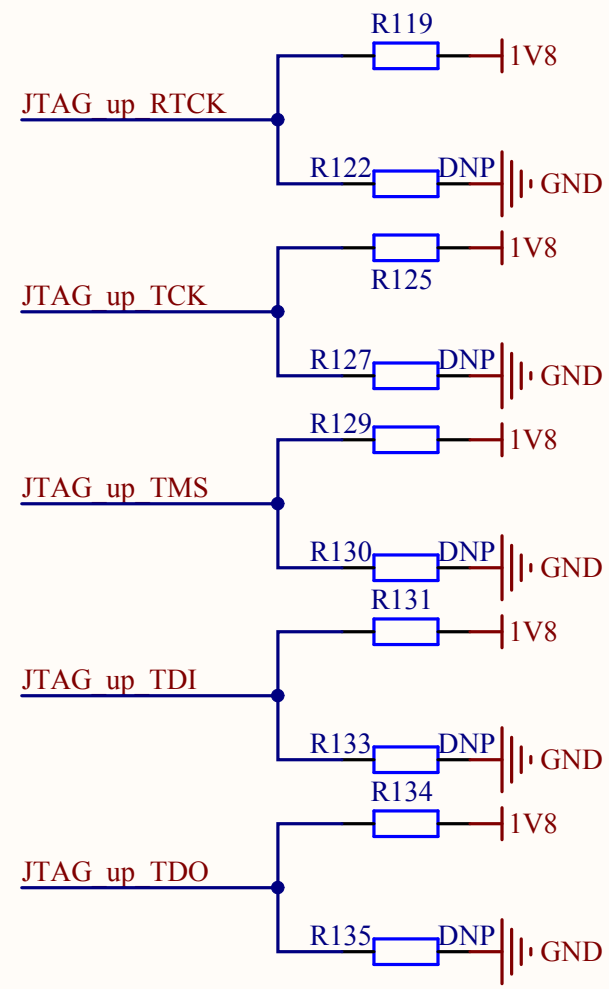


**Ticket 601 - Détrmpneur - Cuper pin 6 sur carte CPU
A mettre dans rapport à L catis (TODO)**

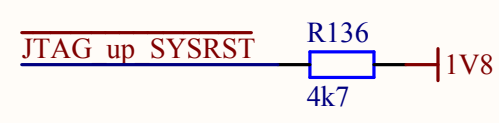
Jtag shared signals Pull-Down



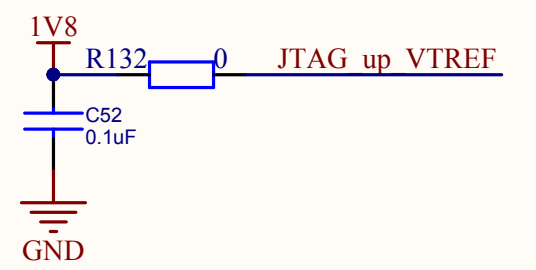
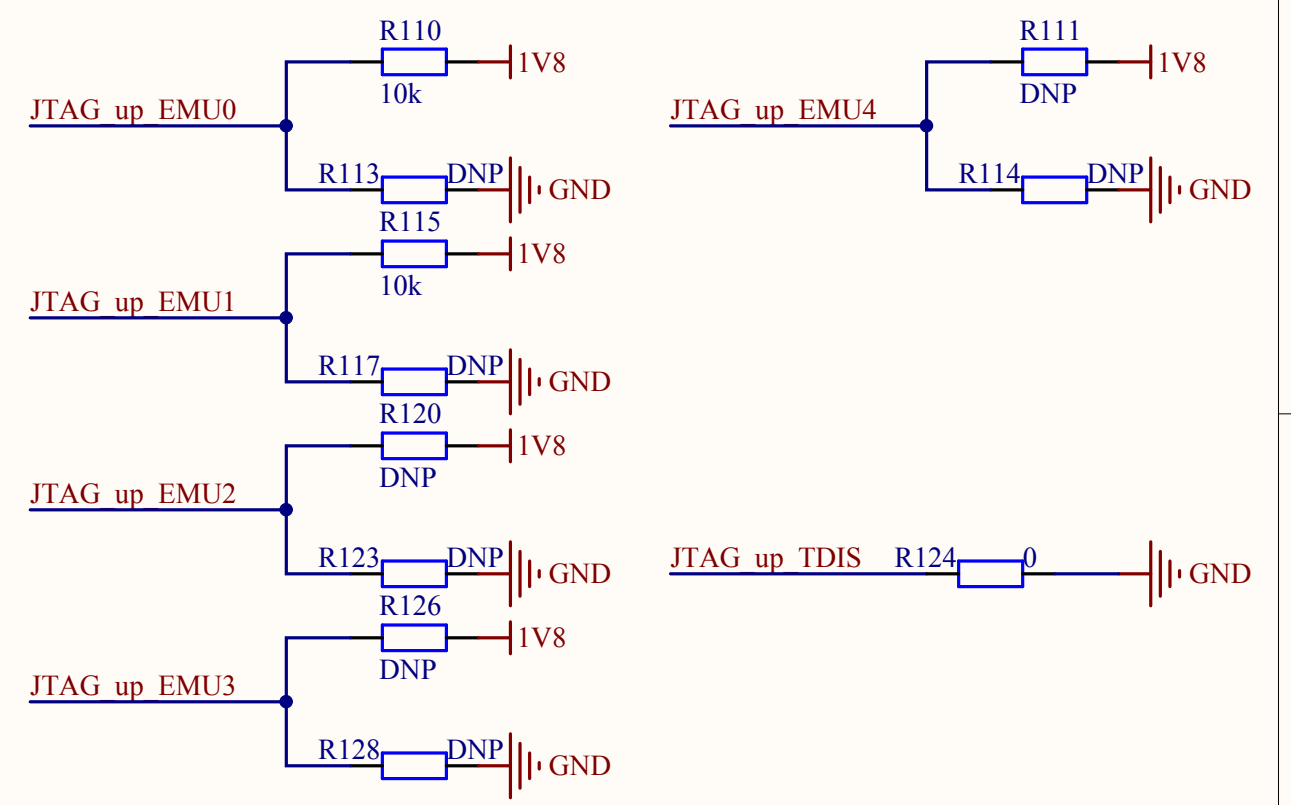
Jtag shared signals Pull-Up



Jtag shared signals



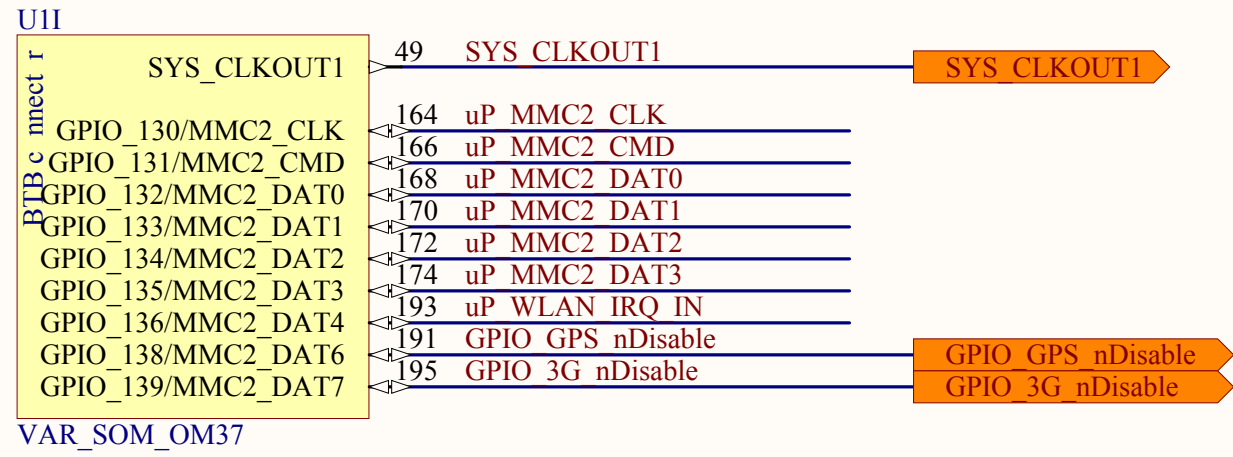
Jtag TI signals



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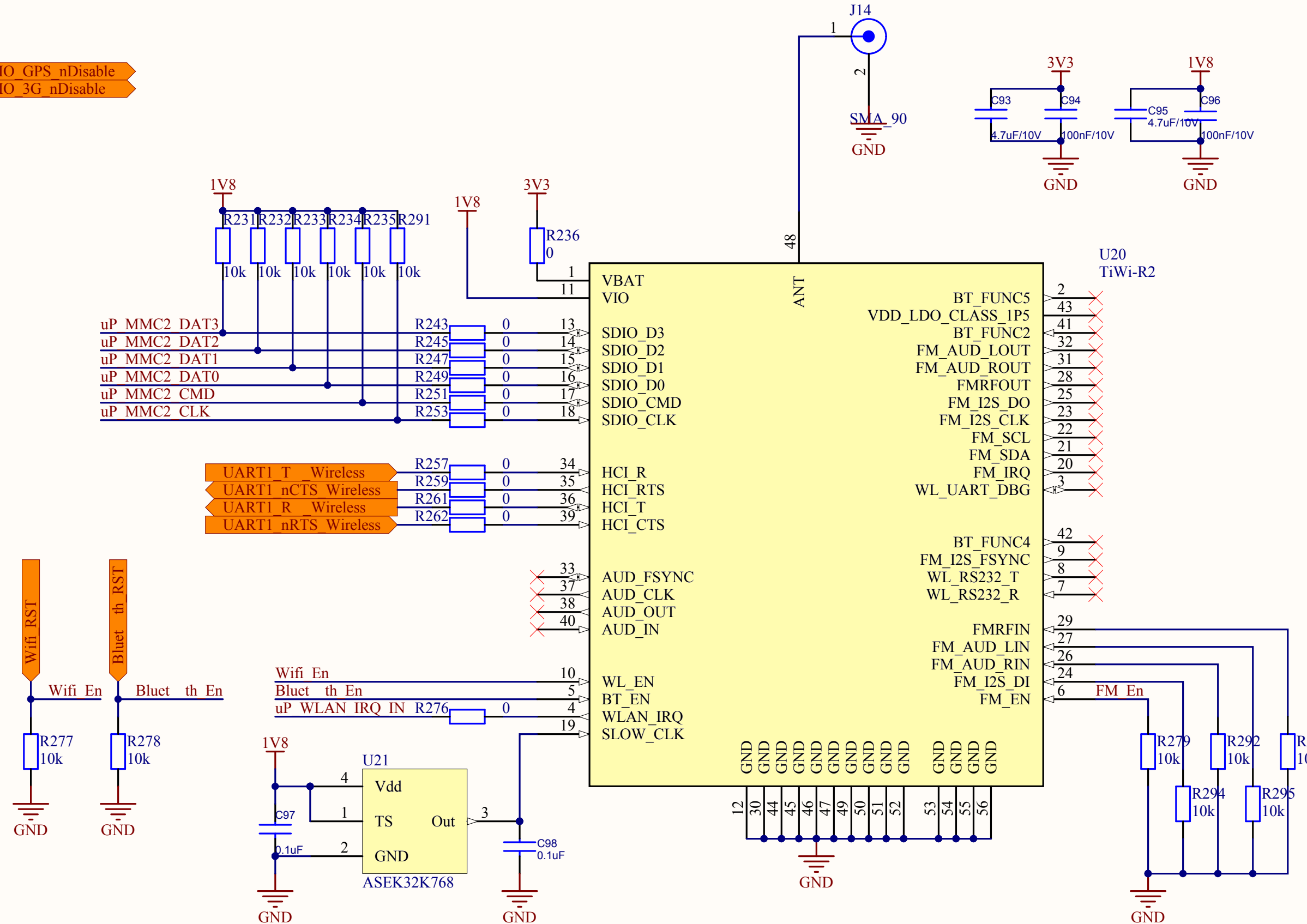


Reds	PCB_DM3730.PrjPCB
DM3730_JTAG.SchD c	
Drawn by: VTT	Rev *
Appr ved by: *	Date: 10.10.2012
	Page * f *

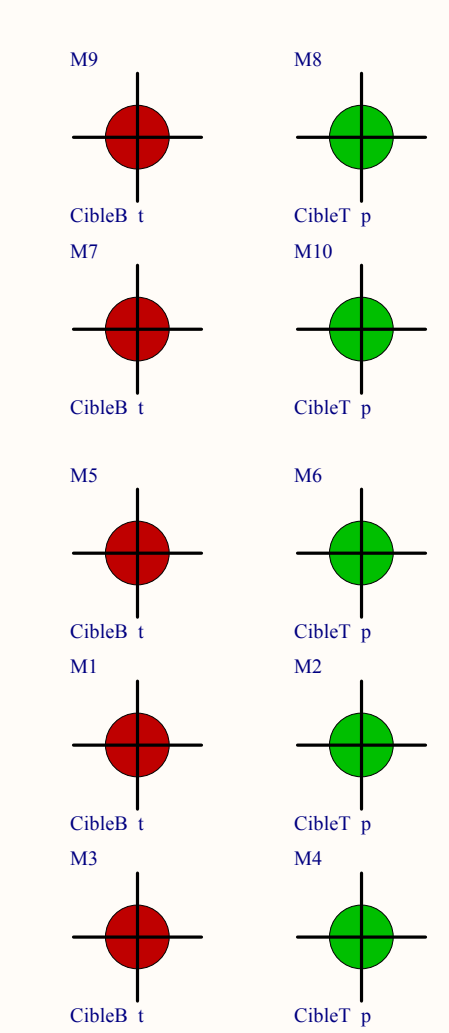
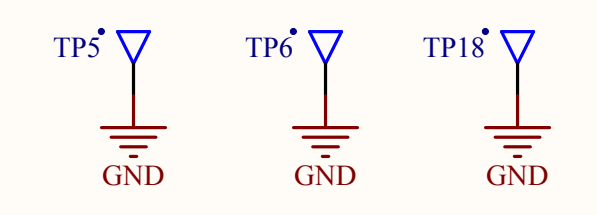
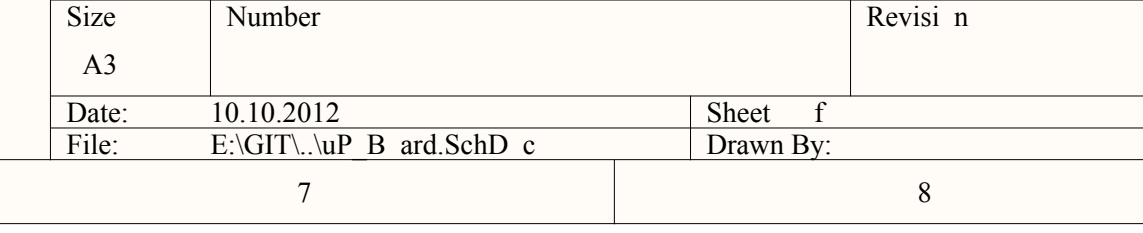
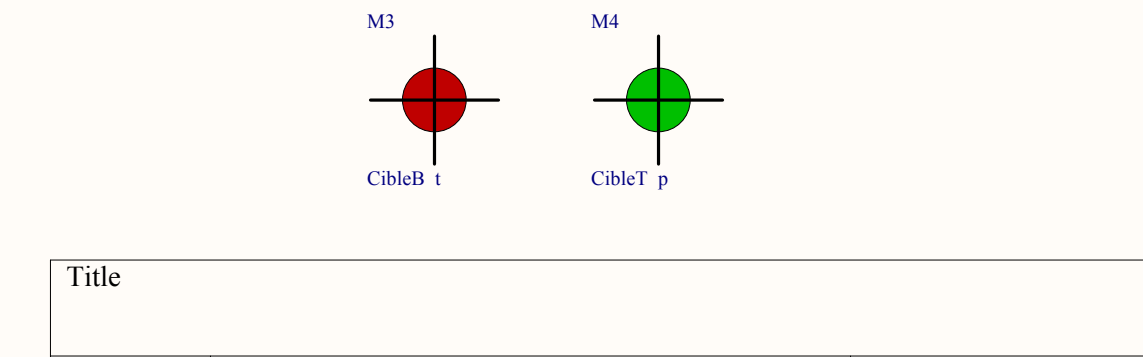
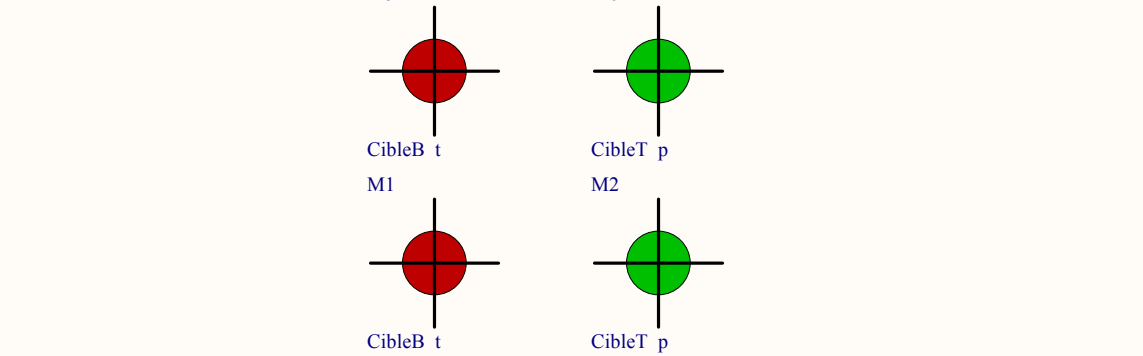
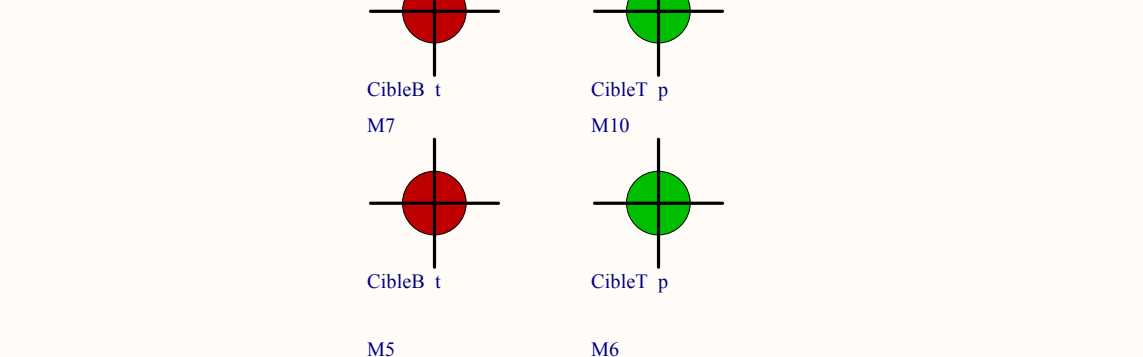
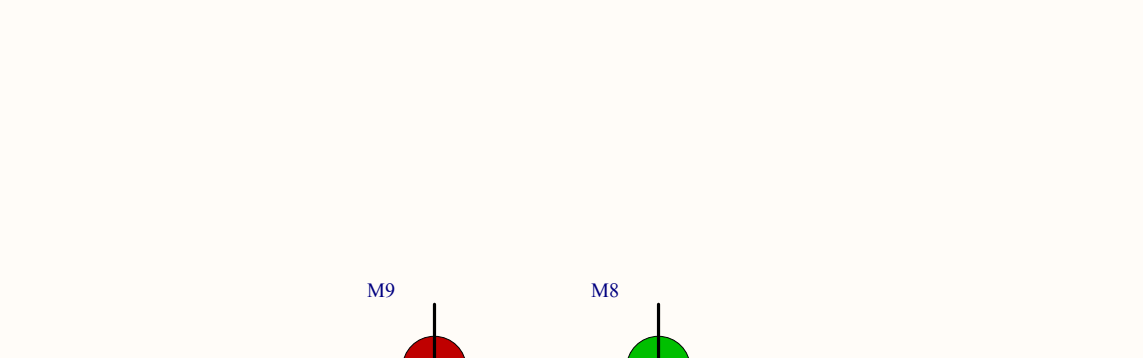
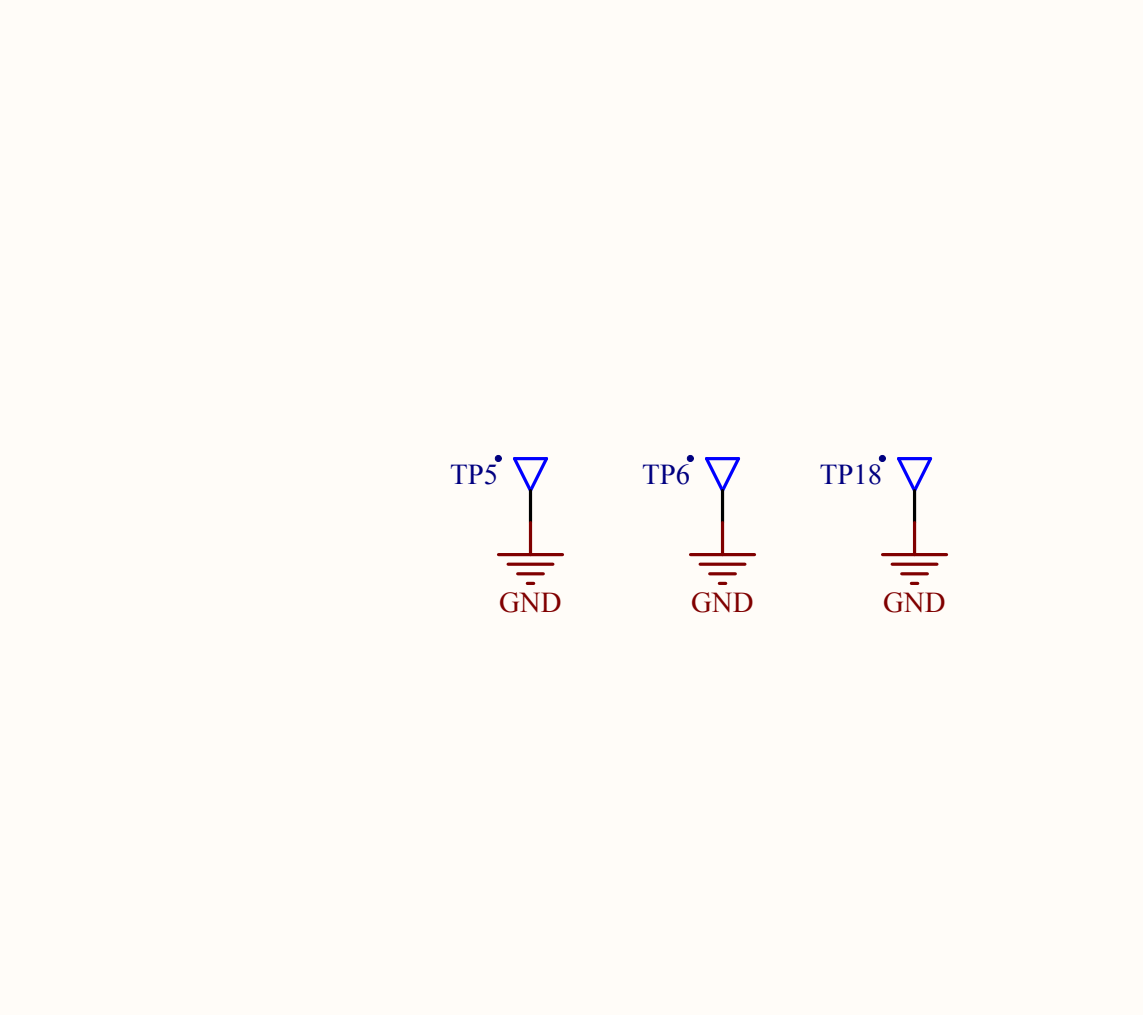
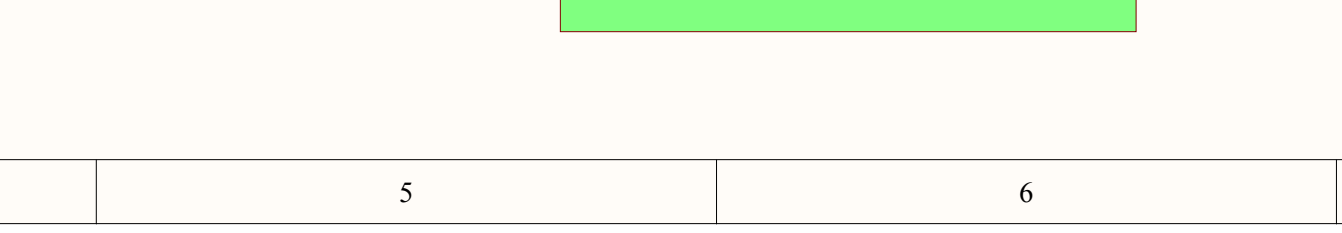
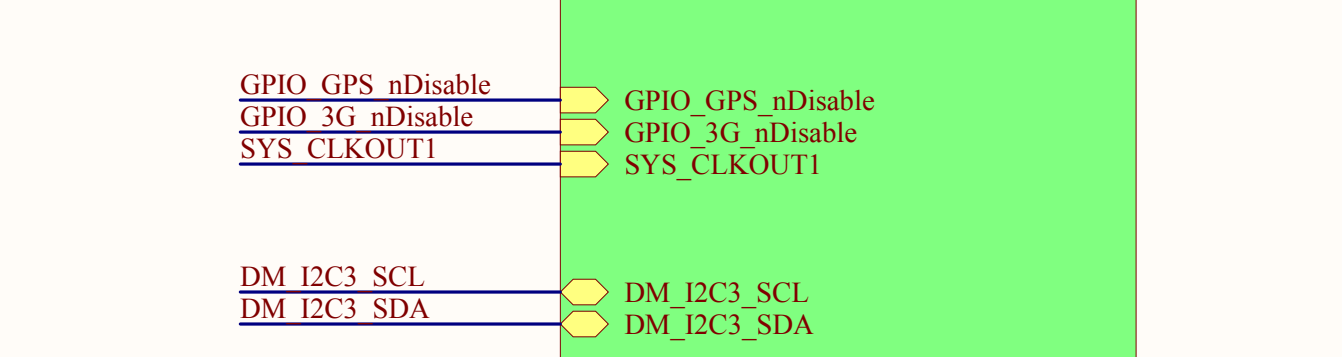
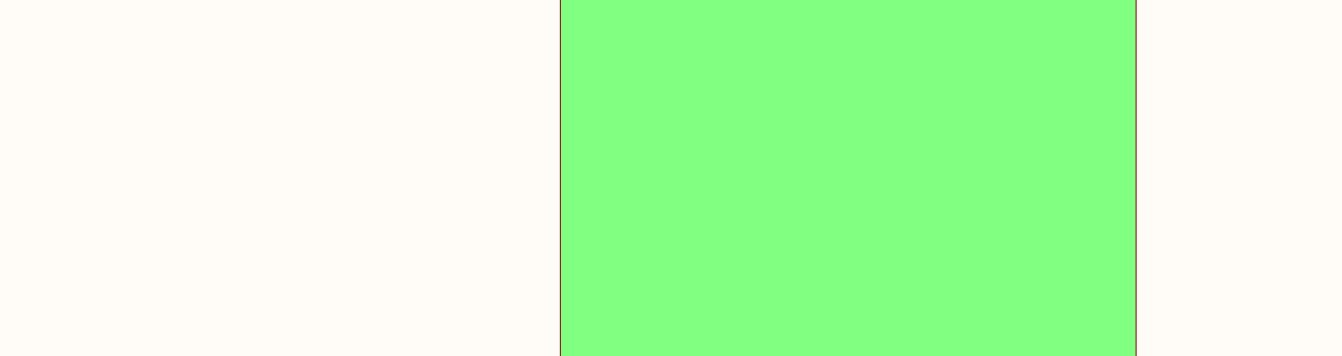
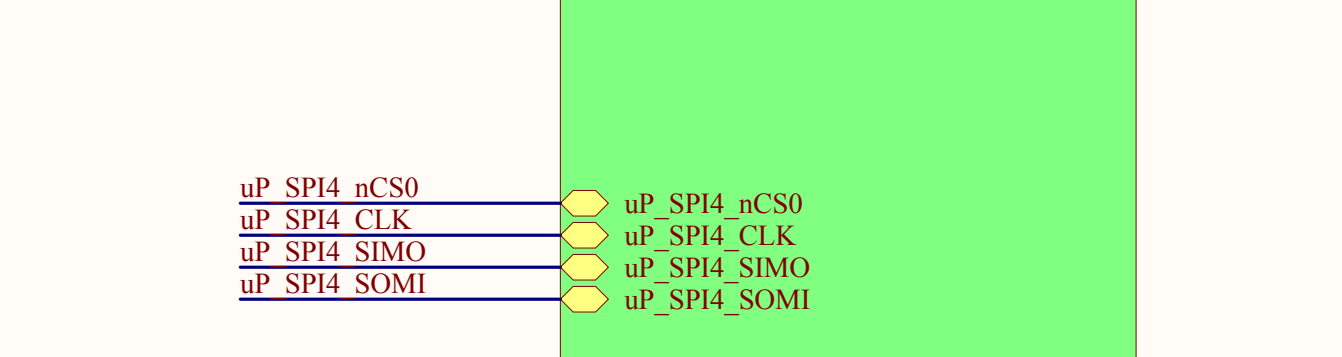
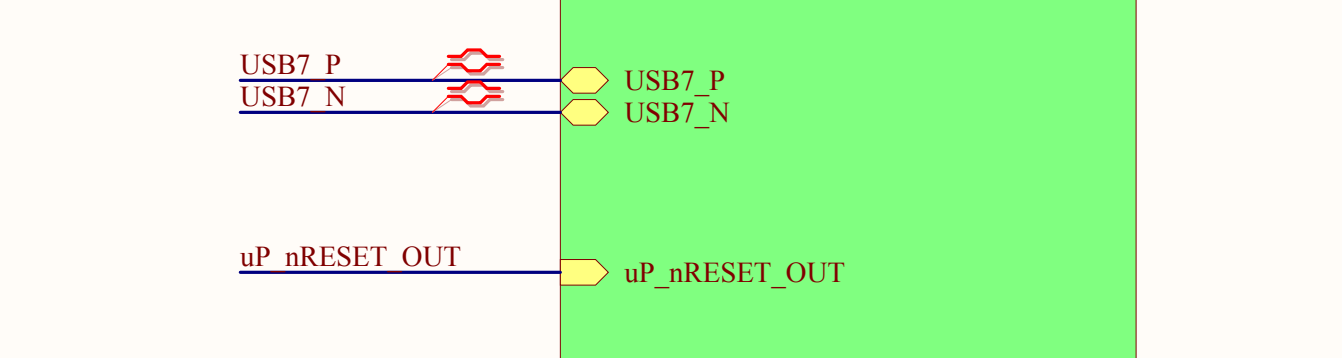
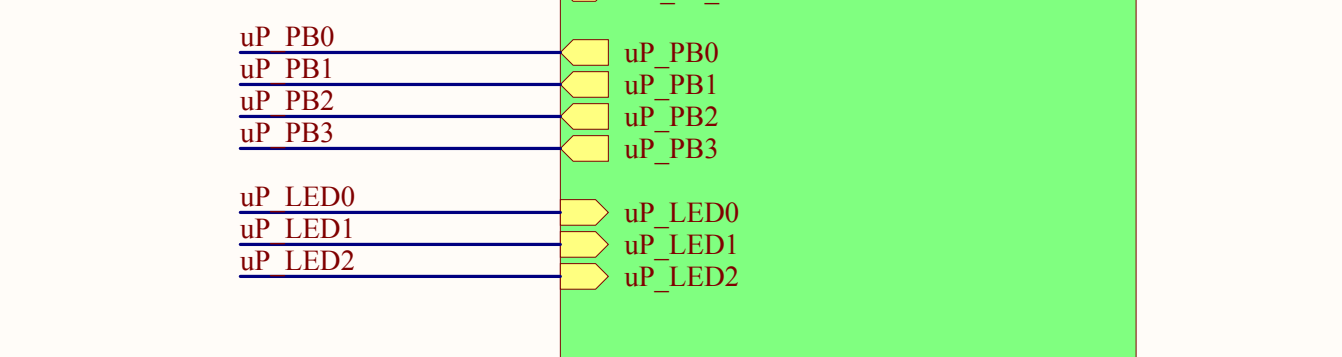
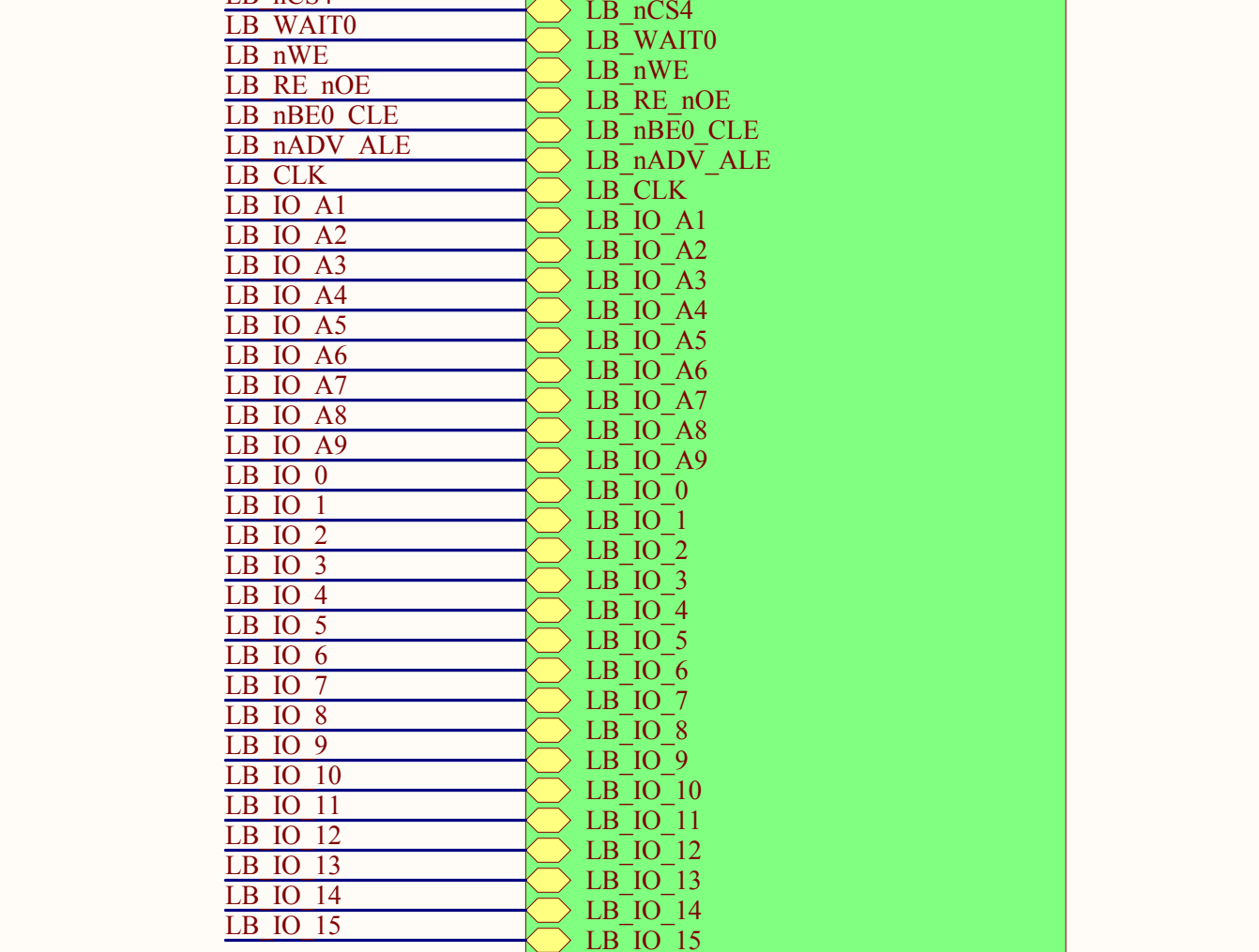
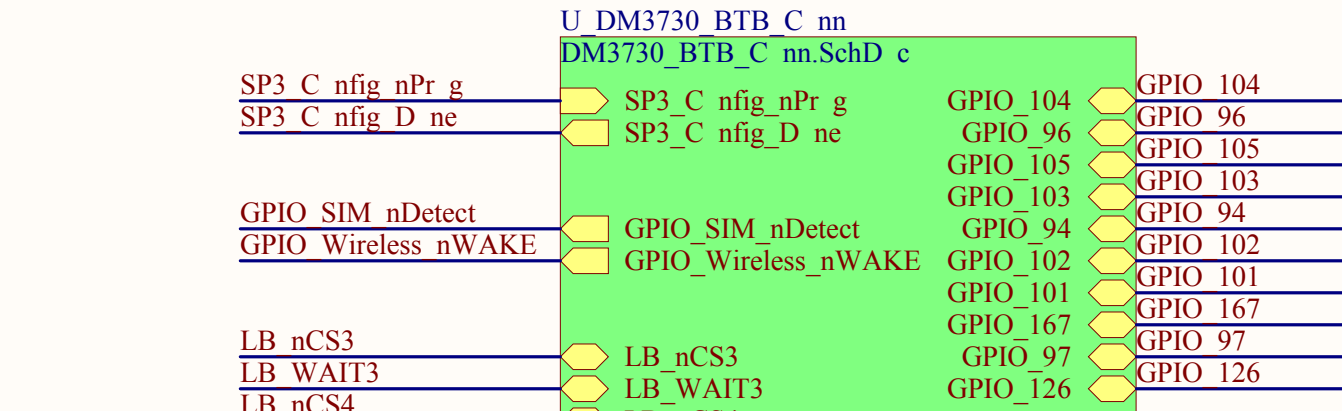
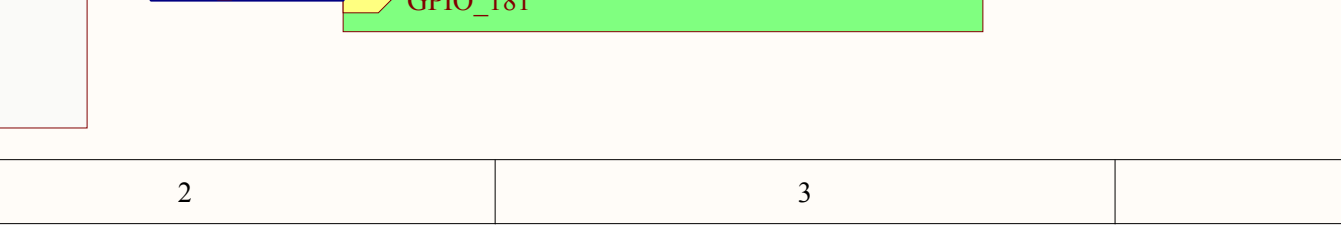
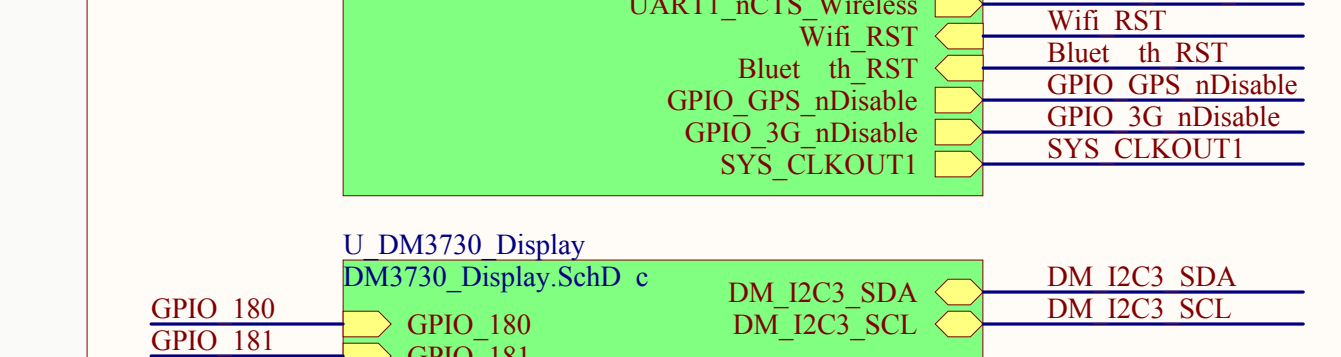
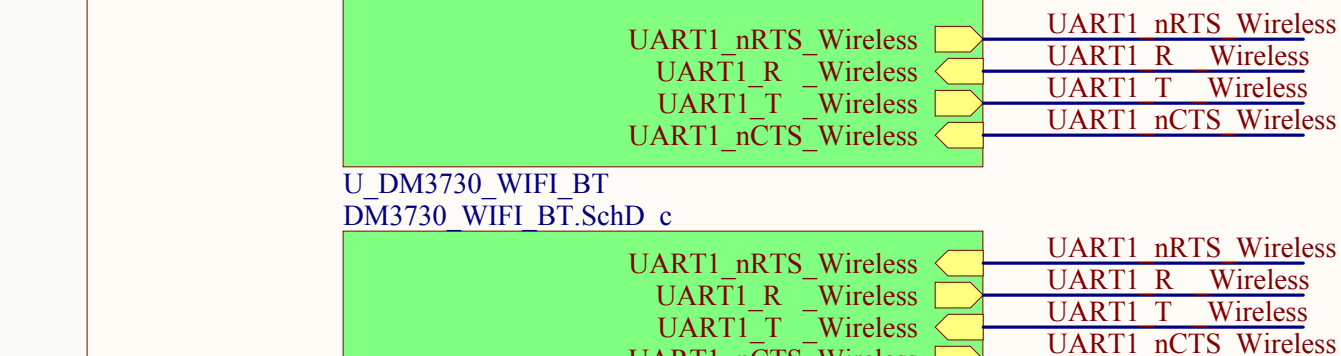
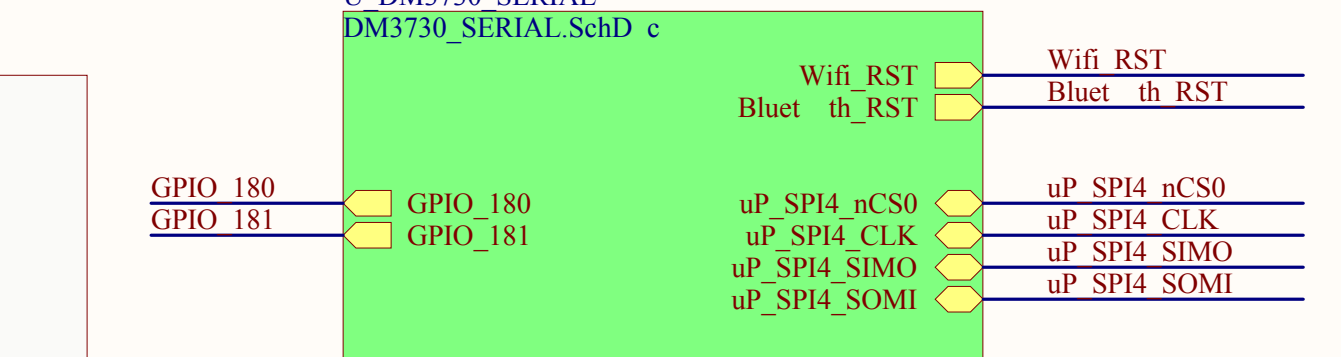
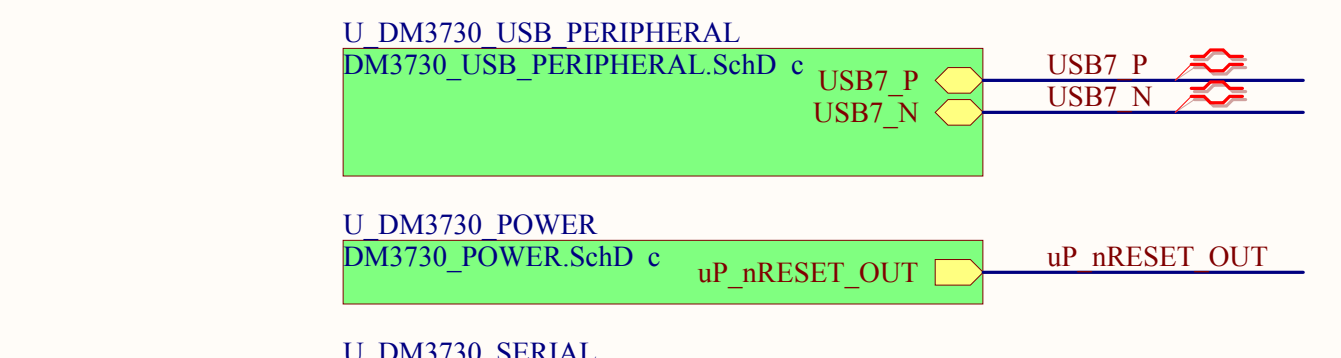
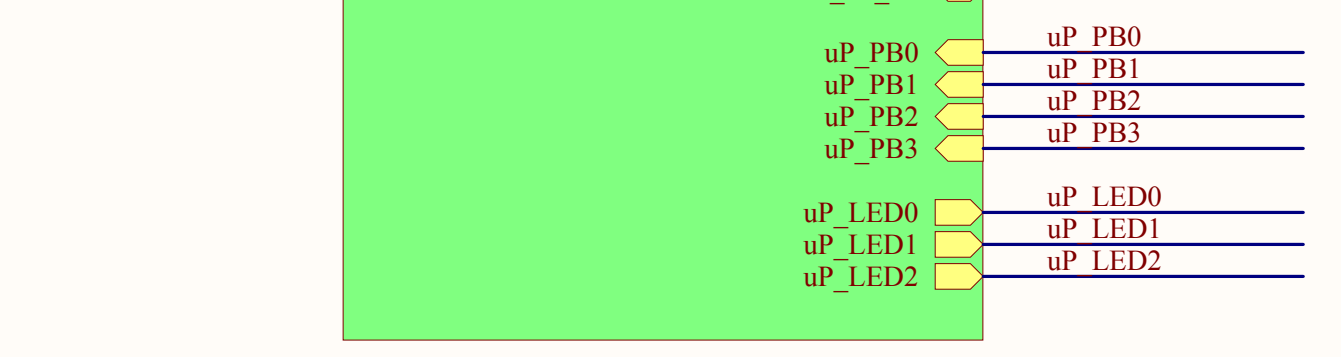
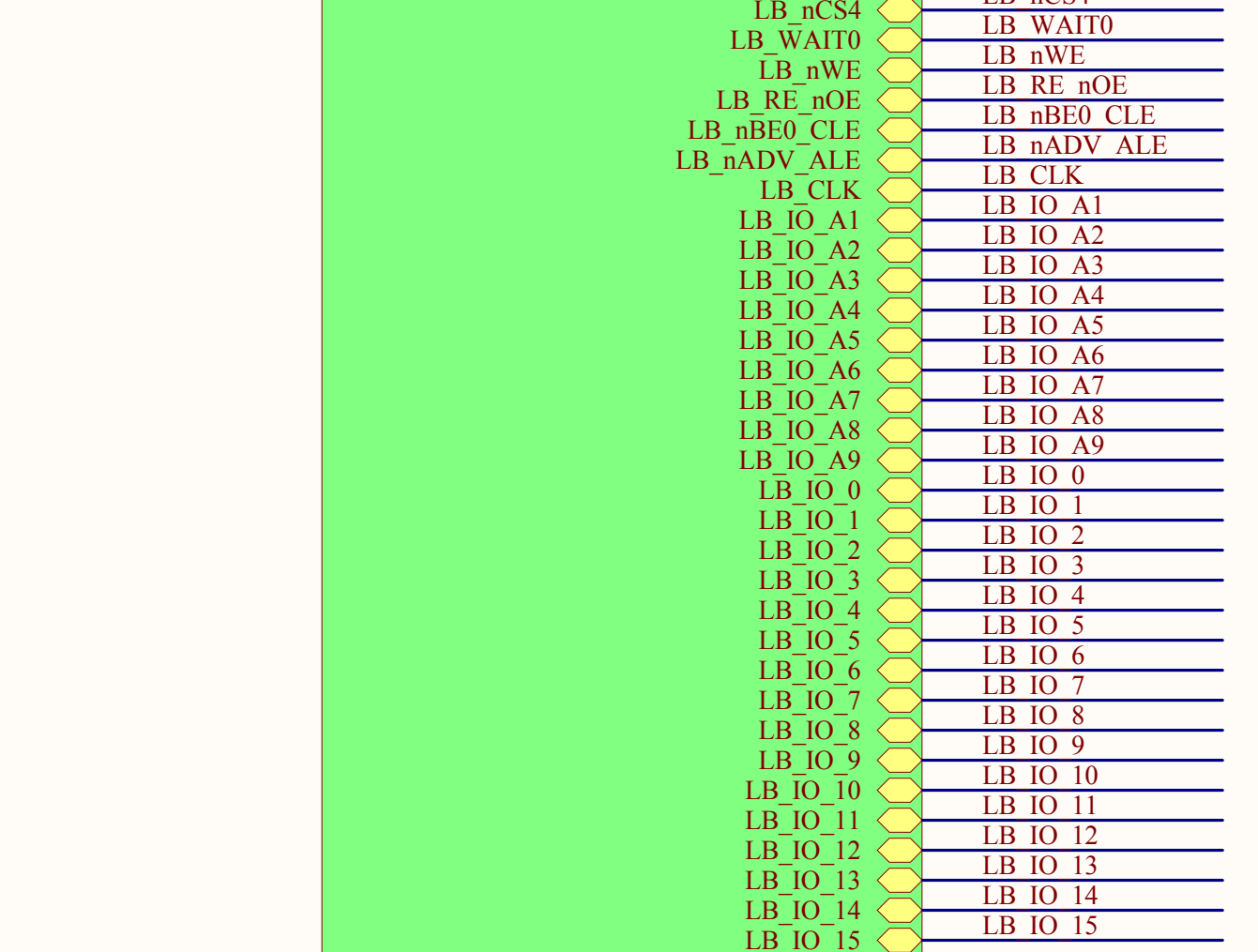
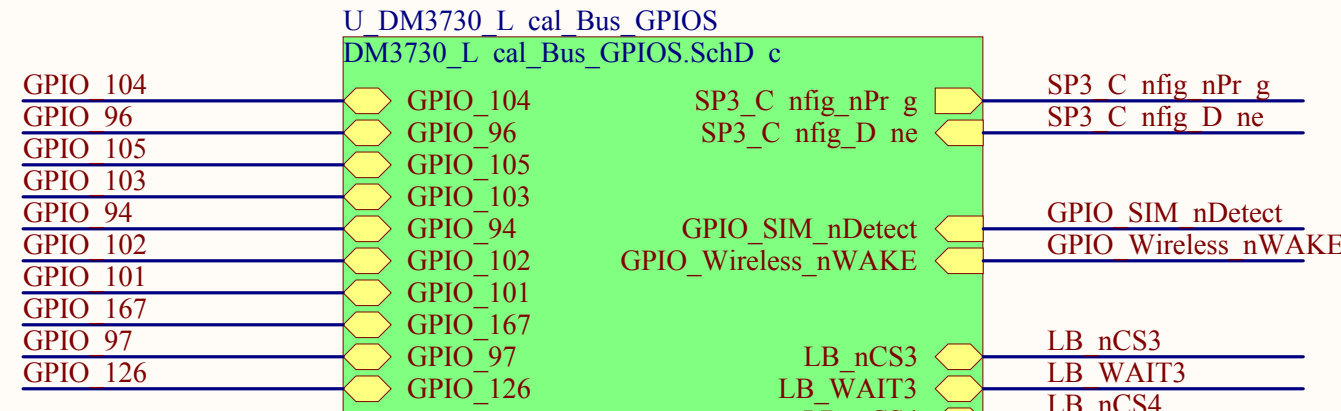
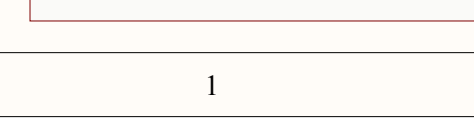
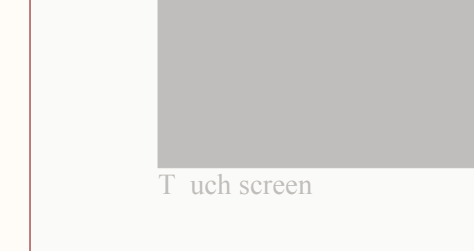
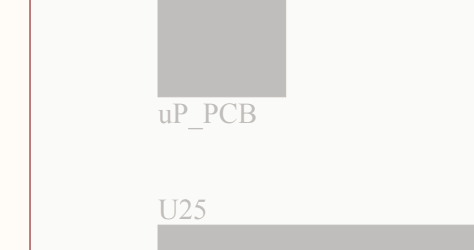
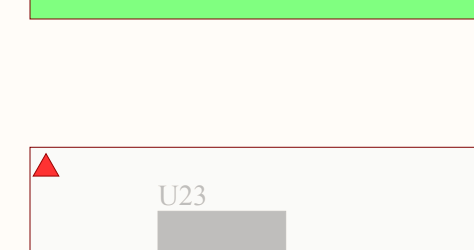
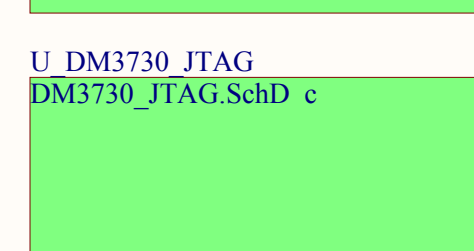
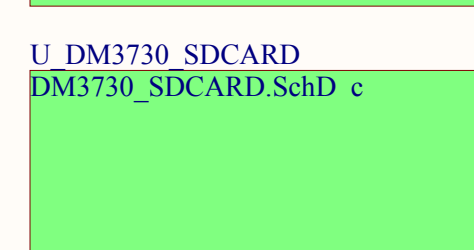
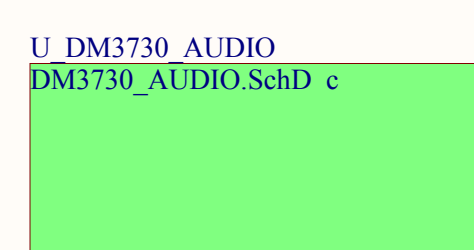
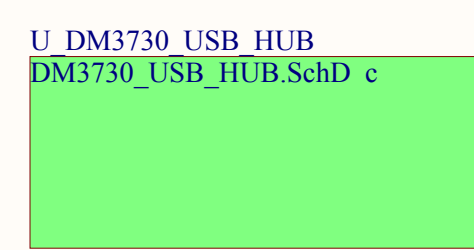
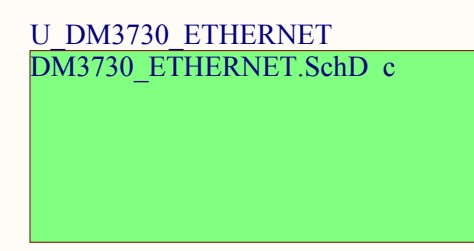
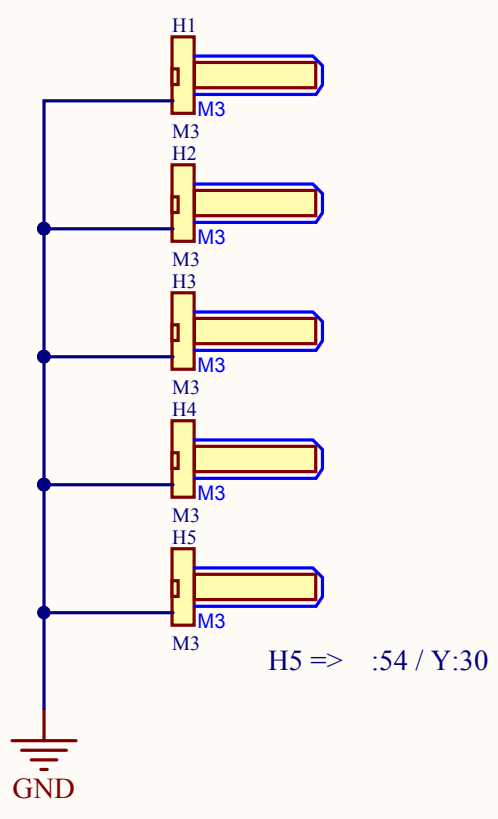


Warning message: "adding items to hidden GND" when doing a compilation is due to hidden pins 3, 4 & 5 of the SMA_90 component.

Revisi n OK 03.10.2012 OAN/VTT



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