heig-vd

Haute Ecole d'Ingénierie et de Gestion
du Canton de Vaud

Reconfigurable & embedded Digital Systems

5 à 7, 1er November 2007

E. Messerli, REDS @ HEIG-VD

HEIG-VD
Institut REDS, Reconfigurable & Embedded Digital Systems
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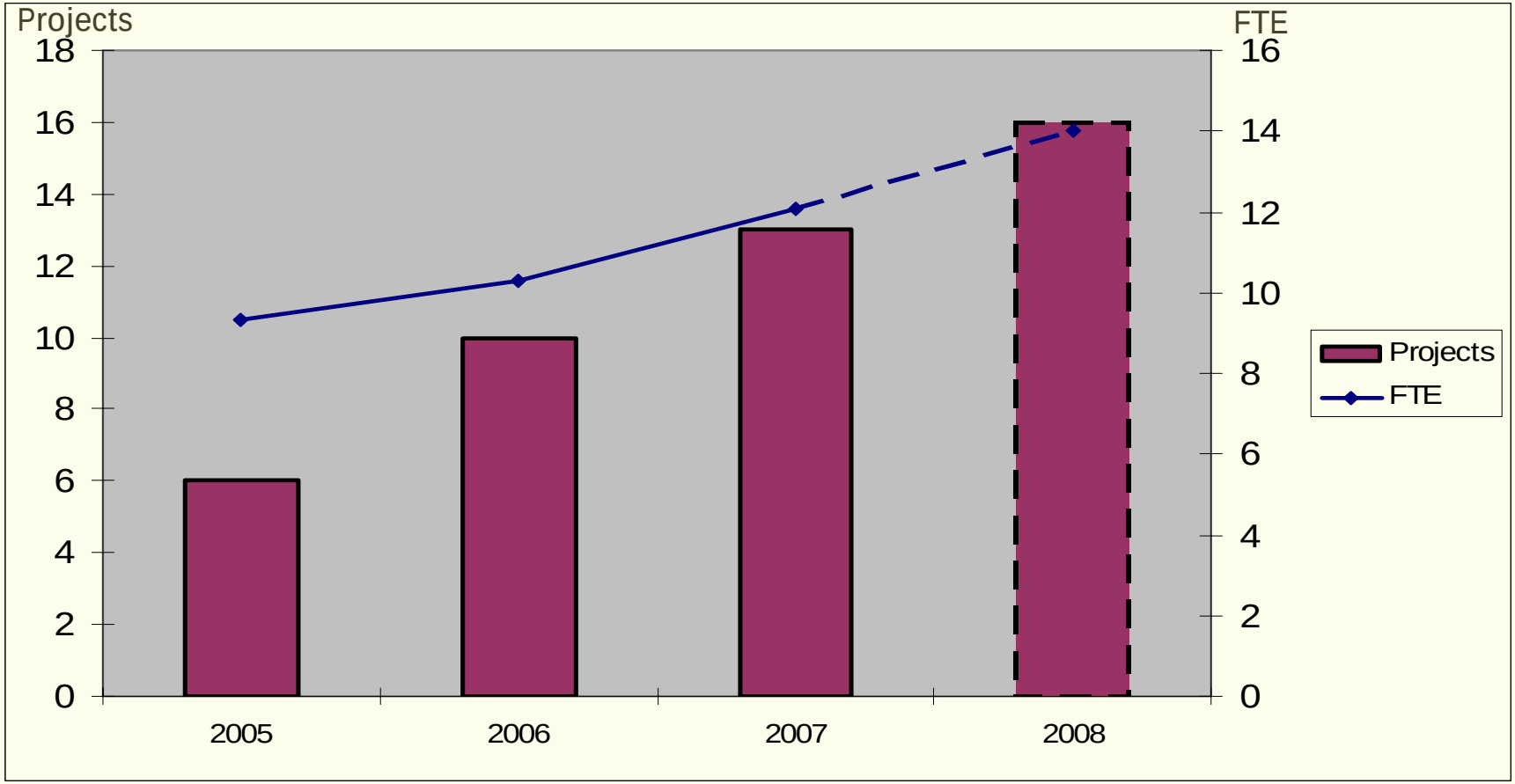
http://reds.heig-vd.ch/

ReDS
Reconfigurable & embedded
Digital Systems

History of REDS

- Created on January 2005
- The institute is young, but already very dynamic !
- It started with 4 professors and 4 engineers
- Now the team is formed by 14 people
  - 6 professors
  - 3 senior engineers
  - 5 junior engineers
- We plan to increase the team on 2008

Evolution of the REDS institute



Projects : number of projects per year
FTE : full-time equivalent

Team, November 2007

- Director
  - Etienne Messerli, professor
- Professors
  - Carlos-Andres Peña
  - Andres Perez-Uribe
  - Daniel Rossier
  - Eduardo Sanchez
  - Michel Starkier
- Senior engineers
  - Olivier Auberson (adjoint)
  - Yann Thomas
  - Andres Upegui
- Engineers
  - Cédric Bardet
  - Guillaume Boutillier
  - Alexandre Corbaz
  - Alexandre Frauche
  - Yoan Graf
- PhD students
  - Miguel Barreto
  - Daniel Jimenez
  - Hector Satizabal

Our vision

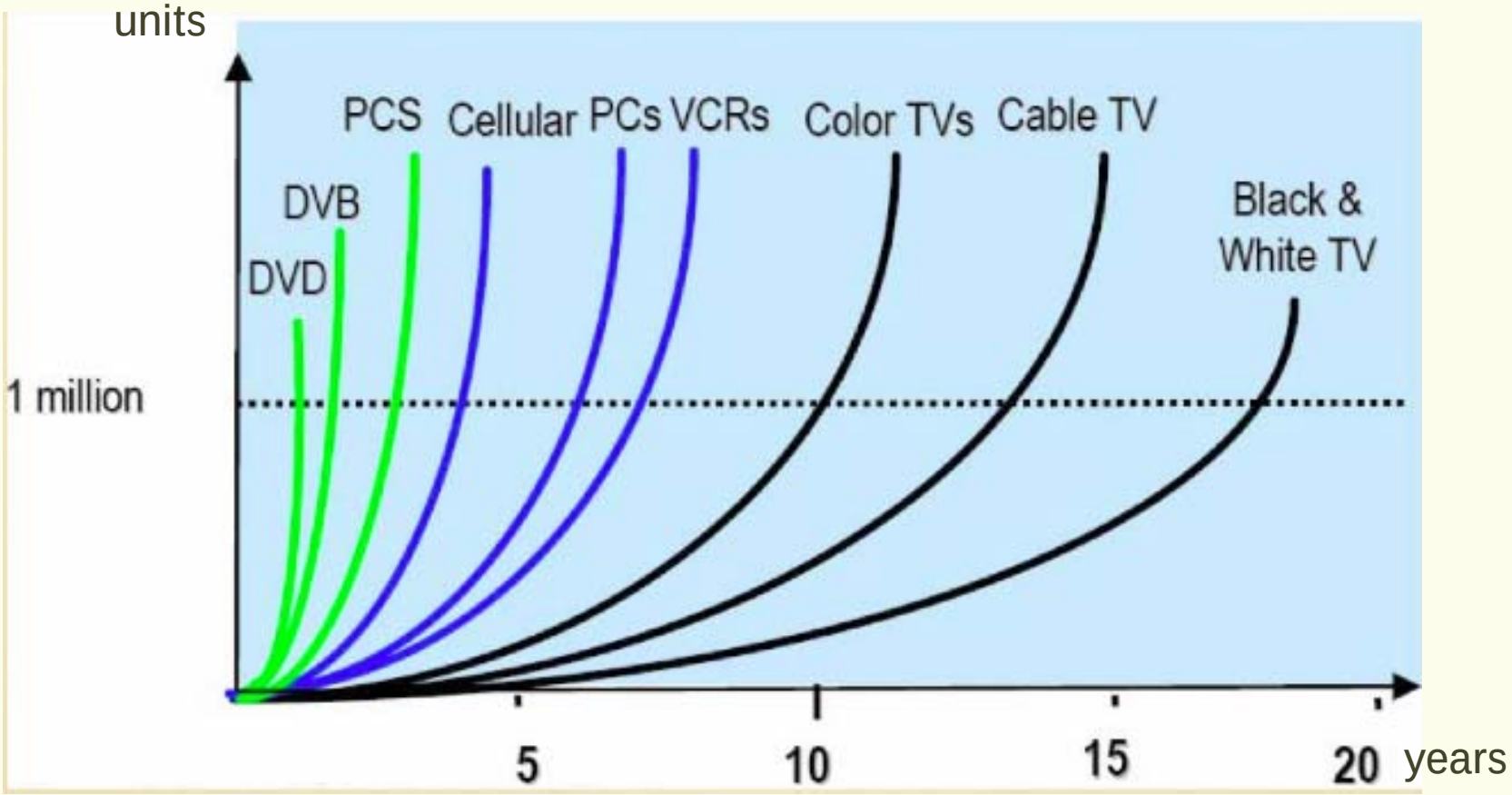
- Evolution of computer information systems
  - mainframes: one computer, many users
  - PCs: one computer, one user
  - embedded: many computers, one user

Our vision: the disappearing computer

"In a near future, the computer will disappear since it will be everywhere: it will be omnipresent, pervasive"

One of our objectives is to be up-to-date and to participate in the development of the technology that will enable pervasive systems to fully interact in a decentralized manner.

Our vision: decreasing time-to-market



Reconfigurable systems based on **FPGA**s offer a solution to the continuously decreasing time-to-market of consumer and industrial digital devices

Our vision: Co-Design, soft vs. hard

Soft

Open SSL-DES with gcc -O3
ARM7 @75 Mhz (~ 20 CHF)

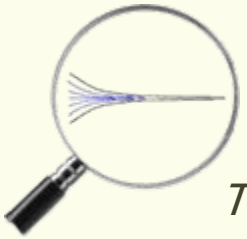
result: 330 µs ⇒ 0.2 Mbits/s

Hard

DES sequential on FPGA
Cyclone II EP2C35 (~ 80 CHF)

result: 240 ns ⇒ 260 Mbits/s

Hard is 1300 faster; with FPGA: gain on ratio speed/price ~300



What is the optimal partition?

The partitioning consists in determining and reducing possible bottlenecks

Areas of expertise

- Embedded digital systems
  - System or board-level design
  - FPGA interface or algorithm implementation (PCI, cryptography, signal processing, ...)
  - OS (eCOS, Linux), RTOS (RTAI/Fusion, Xenomai), middleware, drivers
- Bio-inspired and pervasive systems
  - Design of systems adaptable to the environment and the user using bio-inspired techniques :
    - neural networks, genetic algorithms, fuzzy logic, ...
- Co-Design
  - joint the best partition between software & hardware for each application

Areas of expertise

- Reconfigurable systems
  - dynamically reconfigurable systems
  - pervasive systems
  - automatic system update and reconfiguration (LAN or WLAN)
- Advanced FPGA design for complex systems
  - VDHL language, design methodology, verification methods.
  - re-usable core (IPs), processor-based systems on FPGA (SoPC)
  - behavioral modeling and simulation (Matlab+Simulink)
  - EDA tools (Mentor Graphics tool chain, Altera, Xilinx)
  - vendor independent : Actel, Altera, Lattice, Xilinx ....

Multidisciplinary approach

System level

Signal processing

Cryptography

Bio-inspired techniques

...

OS & Middleware

Open source

RTOS

GNU

LINUX

Drivers

Hardware

CPU 32bits

ARM

FPGA

VIRTEX

Co-Processing & Interface

VHDL IP

Communication

GSM The wireless evolution

Interface

Reconfiguration

Wide bus memory (128, 256, .. bits)

Activities

- Teaching activities (HES engineers)
  - On the areas of expertise
- Postgraduate courses
- Technology transfer and industrial realizations
  - Industrial contracts, coaching, consulting
- Applied research and development
  - Ra&D projects HES-SO
  - CTI projects with industries
  - EU projects, international projects

Teaching activities

- Teaching activities
  - digital systems, computer architectures, microcontrollers
  - embedded systems, operating systems, real-time programming
  - bio-inspired systems
  - programme égalité HEIG-VD : Future ingénieure
- Postgraduate courses
  - Basic VHDL lectures: design, methods and languages
  - Advanced VHDL lectures: design reuse, verification
  - Specific VHDL lectures for company
  - Doulos lectures
    - Expert VHDL, Essential Tcl/Tk, Assertion-based Verification with PSL

Ra&D project partners

- Industrial contracts
  - Bobst (postformation)
  - EM Microelectronic-Marin (postformation)
  - Speedgoat
  - Syderal
- Research projects
  - Armasuisse
- KTI/CTI projects
  - ELCA Informatique
  - Swisscom Innovations
  - NetModule

Ra&D project partners

- European project
  - Wany robotics (FR)
  - UNIL, UJF (FR), UPC (ES), TUL (PL), CNRS (FR), SCIPROM (CH)
- Other international research projects
  - Sécretariat d'Etat à l'éducation et à la recherche (SER)
  - Biotec, CIAT, Universidad del Valle (CO), Ghent university (BE)
- Other Ra&D projects
  - HES-SO réserve stratégique
  - EPFL, SUPSI, CHUV

A team at your service

- Services for industries
  - high tech areas of expertise
  - engineers with up-to-date skills and knowledge
  - high quality of postgraduate courses
  - research projects with public funding (CTI, EU,...)
  - direct contracts
  - multidisciplinary areas of expertise
    - benefit of expertise of several institutes from HEIG-VD

Thank You...


PERPLEXUS
Please wait: booting...
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colibri login: _